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The Front-End Receiver's High Precision Voltage Mode Band Gap Reference Circuit

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Abstract
An essential component of analog integrated circuits' reference voltage generation is the bandgap reference circuit (BGR). The power supply rejection ratio (PSRR), which is utilized to keep the output steady during the transient response, is typically used to represent BGR. Although the BGR circuit is used by receiver front-end transceivers, the system's challenges are thought to be its high-power requirements, sensitivity, complex design, and dynamic range. In order to address the challenges in the system, the Bipolar Junction Transistor (BJT) is added to the Proportional to Absolute Temperature (PTAT) generator cell in order to attain a high factor. In particular, the temperature coefficient (TC) is adjusted for by mutually compensating the first and second-order temperature dependency factors $\boldsymbol{V_{REF}}$*. By adding bipolar transistors, the length of the transistors is utilized to reduce power consumption and limit the impacts of manufacturing variation and mismatches. The starter circuit, Complementary to Absolute Temperature (CTAT), and PTAT generator cell, which sustains the steady output even in the face of transient response, make up the BGR circuit. The region of 1.2V is where the greatest reference voltage was reached.*

Keywords— Bandgap reference circuit, Receiver front-end transceivers, Reference voltage, generator cell, Temperature coefficients.

I. INTRODUCTION

By eliminating surface acoustic wave (SAW) filters, the contemporary radio frequency (RF) front end lowers overall costs [1] [2] [3] [4] [5] [6]. However, because there aren't any high Q filters, the RF front end needs a wide dynamic range. The signal and local oscillator pathways with high power consumption meet strict standards. In order to raise the compression point, current mode techniques restrict the strength in the signal channel. The widespread use of voltage mode circuits in RF transceivers draws attention to their effective compatibility and scaling features [7]. The amplifier is regarded as the essential part of the receiver front-end transceiver, and an electromagnetic radar system is employed for object identification and detection [8] [9] [10]. The low noise amplifier (LNA) effectively processes both strong and weak echoes of the incoming signal. The LNA enhanced the signal-to-noise ratio and high gain when the signal was weak. Because LNA operates at a low gain for short-range objects and has strong linearity and dynamic range, it is possible to prevent receiver chain saturation [11].

High-frequency distortion is compensated for using UPFC circuits, which are utilized in power injection. The UPFC circuits are made up of injection transformers, series VSC, DC link, and shunt voltage source converters (VSC). [12] [13]. Matrix converters take the place of the DC link in direct AC-AC connections [14] [15] [16]. However, the big installation, losses, and limited dynamic responsiveness were the main problems created by the bulky series injection transformer [17][18][19]. Magnetic loss and parasitic resonance cause narrow frequency ranges. [20] [21]. resistive divider and AC-DC converter to create an adaptive biasing (ADB) network.

The ohmic operation of a junction field effect transistor (JFET) is achieved by the employment of resistors. Using the DC load signal from the rectifier, the JFET manipulates the corresponding resistor in the ohmic region [11]. The low-dropout regulator (LDO) is dependent on the reference voltage, which is produced by the CTAT block in analog devices [22]. The ripple voltage of BGRs affects the accuracy of the LDO's output. The BGR approach optimizes the ripple rejection capabilities, and voltage reference accuracy is crucial for the overall functioning of

the circuit. When determining the range of the pulse signals in the Ultra-wide Band (UWB) system, the accuracy of the system is influenced by the RF transceiver's front-end bandwidth (BW). UWB systems have higher requirements for positioning accuracy and communication distance. High sensitivity, transmitting power, and dynamic range are required for both sending and receiving routes. The intricacy of the bias and control circuits in the transceiver front end design makes integration more challenging [23]. Multiple RF frontends raise the BW of the entire channel, increasing system cost and power usage [24]. The direct sampling receivers (DSR) prevent analog mixing problems such as reciprocal mixing [25], harmonic down-conversion [26], and picture concerns [27].

However, to lessen the problems with noise folding and aliasing, tunable RF filters are needed [28] [29]. The filter must loosen the jitter requirements because the sample pulses are generated by the Phase-locked Loop (PLL) [30] [31]. The multi-transistor used in adaptive biasing circuits takes up a lot of space, and the circuits' low precision and intricate design are regarded as drawbacks. Although the complexity structure is unsuitable for deploying the discrete circuits, the gain is adjusted using a Gillbert-cell-based topology [11]. The PTAT generator cells in this study are connected in series to add up the distinct currents and voltages. The voltage reference temperature is compensated by temperature dependency of the first and second orders. Lastly, to attain a high K_i factor, BJT is added to the PTAT generating cell. The CTAT temperature dependence V_{CTAT} is matched by increasing the PTAT temperature dependence term V_{PTAT} due to the transistor layer.

By adding the BJT, the transistors' length is utilized to limit the effects of production variations and mismatches, which in turn lowers power consumption. The design of the BGR circuit with a single BJT branch to achieve the stable reference voltage is the primary contribution of the study.

II. LITERATURE SURVEY

The literature review section discusses current approaches and their drawbacks. The CMOS BGR circuit, created by Trang Hoang *et al*. [7], was utilized to maximize the PSRR, a measure of the circuit's capacity to sustain a steady output. The algorithms maximized the differential gain to maximize the PSRR, and current source blocks were used to improve the bias accuracy. To keep the rotational angular speed constant, weight parameters were used. To reach the PSRR value, the TC parameter must, however, surpass its limitations.

Haishi Wang *et al*. [24] introduced the mixer-first receiver, which uses baseband noise elimination to lower power. The wide bandwidth and filtering profile were made possible through the manipulation of pole and zeros locations using capacitive feedback. Analog receiver performance for high-data transmission at low and high power levels. However, because of the infinite bands, the noise cancellation technique offered ineffective pulse transmission.

The improved beta multiplier was incorporated into the bandgap reference circuit, which was introduced by R. Nagulapalli *et al.* [33]. The NMOS transistors' fixed resistors were moved, and PMOS transistors reduced the mismatch. Utilizing the reference circuits, which take up less space, decreased power consumption. Large body effects, however, caused mistakes in CMOS technologies.

Using the lower power components, Mowei Lu *et al.* [21] created the power flow and quality control structure. The power supply was supplied via shunt and series converters with high-frequency interconnections, and the ground connections were avoided by using floating modules. In order to achieve the high power and frequency, compact size, and volume, bulky and dynamic line transformers were not used. However, in meshed grids, the power flow control method is the primary cause of unregulated power flow, which results in overload problems.

III. MOTIVATION

The BGR circuits are essential for producing the reference voltage (VR) in analog integrated circuits. The PSRR, which sustains a steady production, determines BGR ability. The overall performance of the circuit was impacted by variations in the supply. However, the power electronics devices' accurate current sensing enhances the protection, control, and reliability mechanisms. Because of the limited device storage in wide band gap semiconductors, the current sensing approach makes monitoring the different currents more difficult. Therefore, in order to offer a consistent reference output voltage, the BGR circuit design needs to be changed.

IV. CHALLENGES

This section examines a number of issues with the current approaches that the suggested Bandgap reference circuit

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resolves.

- The feedback loop's stability is guaranteed by a multistage amplifier, which calls for big capacitors and bias currents for compensatory purposes [2]. By ignoring the high-order effects, equation-based approaches decreased the efficacy of analog circuit design [7].
- The second stage circuit had to compensate for the high-frequency gain since the cascade circuit in the c-band receiver circuit integration was more sensitive. The receiver circuit's out-of-band suppression was improperly constructed. [23].
- To achieve the huge gain, a large miller capacitance was needed, and differential signalling was needed at the Transimpedance Amplifier (TIA) to lessen the impact of common mode noise [32].

V. SYSTEM MODEL OF BANDGAP REFERENCE CIRCUIT

The semiconductor bandgap, which takes into account the particular circumstances to provide a stable output voltage at a certain value, is proportional to the bandgap VR. The temperature affects the semiconductor's physical characteristics, hence it also affects the output voltage. The modest temperature dependency of charge mobility carriers in Si semiconductors leads to the adoption of bandgap voltage reference circuits. A three-terminal device called the BGR circuit is used to lessen variations in potential differences. In BGR circuits that are nonlinear, a high supply voltage causes a slight variation in VR. The BGR voltage source is designed using two elements with distinct TCs. Transistors, op-amps, and/or diodes make up BGR circuits.

The BGR circuit is made up of current mirrors and a steady current source. The current mirror uses two PNP transistors to control the current. The output VR is provided by two transistors that are positioned at the bottom. The VR and the voltage drop between the transistor Q2 and resistor are same. When the base-emitter current flows via a forward-biased diode, the transistor travels linearly, and the overall voltage drop in this area is proportional to the bandgap. In the BGR circuit, the resistor has a positive TC and the transistor has a negative TC. When selecting the opposing TCs of the components, the resulting VR has 0 TC. Figure 1 illustrates the system model of the BGR circuit.

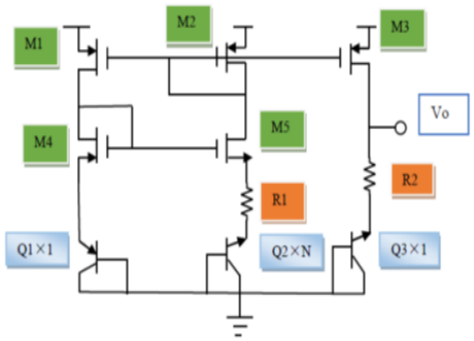

Figure 1 Bandgap Reference Circuit System model.

A. Proposed Bandgap Voltage reference using single Bipolar Junction Transistor Branch

Each transistor in the bandgap voltage reference circuit has a threshold voltage level above 0.6 V, which is utilized to activate the gate-source voltage. The starter circuit receives a reference current. Low leakage current aids in fully shutting off the startup circuit during CR (Current reference) operation. The trimming circuit is added to the CTAT circuit to offset the mismatch effects caused by the PTAT Slope if the circuit rises above the threshold level. Startup problems are lessened since a large percentage of PTAT cell transistors are grounded. By adding BJT transistors at the last layer of the circuit design, the power consumption is decreased and the temperature dependency coefficients are increased.

Transistors' length is utilized to reduce the effects of process variation. At various stages of the operation, the BJT transistor's base-emitter voltage is less impacted. To account for the TCs, temperature dependency terms of the first and second orders are employed. The second-order effect of V_{CTAT} and V_{PTAT} optimizes TCs.

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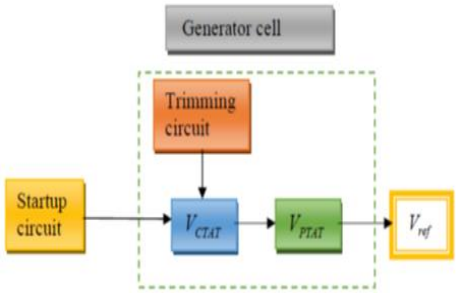

Figure 2. Block schematic of suggested Bandgap Reference Circuit

B. Architecture of Bandgap Reference circuit

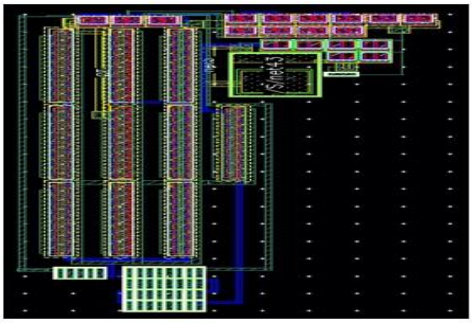

Figure 3. Bandgap Reference circuit Architecture

By preserving symmetry, the BGR layout configuration uses the least amount of space possible, preventing mistakes and inconsistencies. The layout design makes use of smaller, interconnected component units. The bandgap reference circuit's area is. Each component's layout is created using the Layout vs. Schematic (LVS) and Design Rule Checking (DRC) guidelines. By filling the gaps between the components, the decoupling capacitors (DECAPs) in this arrangement help to lower circuit noise. DECAPs are made with NMOS transistors, while PMOS transistors are employed for low leakage applications. The ground is connected to the NMOS transistors that round the guard ring. The supply voltage, which polarizes the transistor bodies, is coupled to guard rings. The BGR circuit architecture of the RF frontend transceiver is shown in Figure 3.

C. Startup circuit

Low voltage CR is used in the startup circuit to lower power consumption, and the biasing circuit is necessary for the transistors to function in the sub-threshold area. $2nA$ is the range of the reference current value. Each transistor in the startup circuit region activates the gate-source voltage to fully start the circuit when $V_{TH} > 0.6V$. Additionally, the starter circuit in the CR operation is turned off using the low leakage current. PMOS and NMOS transistors are used in the starter circuit to convert the zero current area into a typical working zone. The BGR circuit's regular behavior is altered in the herbinate mode by using every transistor in the starting circuit.

D. Complementary to absolute Temperature voltage.

The circuit's PNP transistor Q1 is designed to produce the base-emitter voltage needed to determine the circuit's CTAT voltage. The circuit's voltage divider is attached to transistor Q1. The $\boldsymbol{V_{CTAT}}$ is produced by converting the high voltage into a tiny voltage in accordance with the voltage rule. One way to write the mathematical expression is,

$$V_{CTAT} = \frac{V_{BE}}{3} \qquad (1)$$

where V_{BE} is the PNP transistor's base-emitter voltage. To mitigate the effects of the load, a unity gain buffer is added to the divider, using the 2nA current range. The capacitance is added to the buffer to keep it stable. To account for the temperature, the V_{CTAT} can be used to compute the first and second order temperature dependent terms. The resulting mathematical formula is as follows:

$$\frac{\partial V_{CTAT}}{\partial t} = \frac{V_{be} - V_{BGR} - \beta V_t}{3t} \qquad (2)$$

$$\frac{\partial^2 V_{CTAT}}{\partial t} = \frac{1}{3}\left(\frac{1}{t}\frac{\partial V_{be}}{\partial t} - \frac{V_{be}}{t^2}\right) \qquad (3)$$

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where V_{BGR} is the bandgap VR and $'t'$ is denoted as the temperature. The collector current is used to modify the temperature dependence of the CTAT.

E. Trimming circuit

To address the output fluctuation in the various corners, the circuit design incorporates a trimming circuit. Implementing the trimming circuits fixes the process fluctuations and device mismatch circumstances that reduce output voltage accuracy. By modifying the aspect ratio k_a, the trimming circuits are utilized to maximize the TC. The trimming circuit's design can be represented as follows:

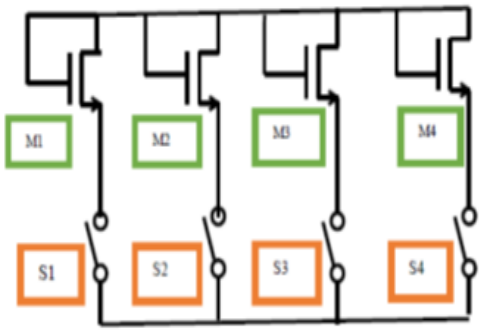

Figure 4. Schematic of Trimming circuit.

The trimmer circuit modifies the PTAT slope to maximize TC by combining four transistors and four switches in series. For each sample in the VR measurement, the mean of TC is lowered in the trimmer circuit. The TC of the output current and voltage determines how the supply voltage varies. Figure 4 shows a representation of the trimming circuit.

VI. RESULTS AND DISCUSSIONS

Effective post-layout and pre-layout findings are provided in this results and discussion section to demonstrate the circuit's effectiveness.

A. Experimental setup

To implement the BGR circuit, the PSpice/LT Spice platform is utilized. LTspice software's analog electronic circuit simulator is utilized in linear technology, analog device, and maximum integrated source models. In order to save time and money, complicated equipment designs are created by simulating complex mixed-signal systems using PSpice software.

B. Post layout results

The system's post-layout outcomes are derived from the simulations, and the layouts are extracted from the simulations using DRC and LVS.

1. Startup voltage

The output voltage of V_{CTAT} generation is determined by the BGR circuit's startup time. According to Figure 5, the supply voltage stays steady at 3.3V between 200 and 500 µs by increasing linearly from 100 µs. Meanwhile, the voltage is generated by the V_CTAT at 130 µs, and it climbs linearly to 200 µs afterwards. In the region of 1.2 V, the V_{CTAT} keeps the bandgap VR steady at 200µs. From 200 to 500 µs, this voltage keeps the output steady. Figure 5 shows the voltage upon starting.

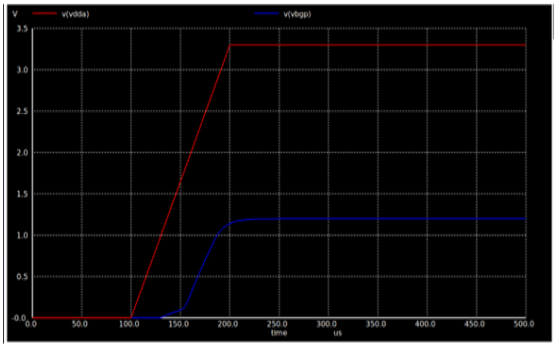

Figure 5(a). Characteristics of Startup voltage

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2. Bandgap VR

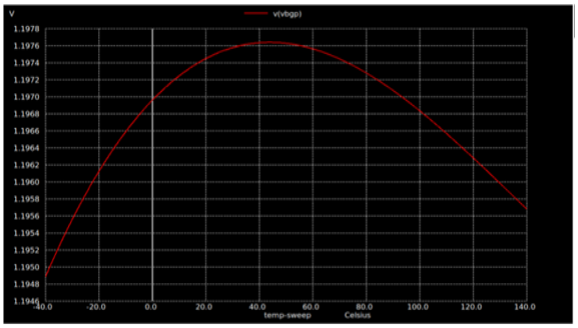

Figure 5(b). Characteristics of reference voltage

In order to create the VR, Bandgap VR balances the positive and negative TC. Temperature is taken into account in the post-layout simulation results between -40°C and 120°C, and the VR reaches its maximum voltage at these temperatures. When the temperature was -40°C, the VR reached 1.1949V. At a temperature of 40°C, 1.9676V is reached, which is regarded as the highest VR level. Following that, the VR drops linearly with less fluctuation between 60^0 and 120^0C. Figure 6a shows the bandgap VR waveform, and Figure 6b shows the bandgap VR in the corners.

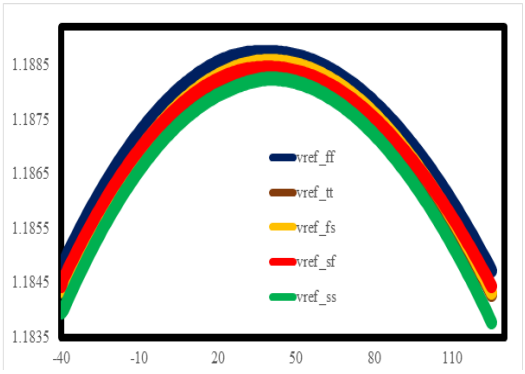

Figure 6. a) Bandgap VR, b) Bandgap VR in corners

3. Supply frequency Vs temperature sweep

The components that create the VR dependent on temperature are PTAT and CTAT. In the BGR circuit, raising the temperature causes the PTAT voltage to rise and the CTAT voltage to fall. To cancel the change in voltage drop, these components are connected in series and their settings are adjusted. Regarding the temperature range of -40^0 C to 120^0 C, V_{CTAT} in the BGR circuit drops linearly from 0.81 V to 0.50 V. Furthermore, depending on the temperature range of -40^0 C to 120^0 C, the V_{PTAT} grows linearly from the 0.39V to 0.70V range. The bandgap VR of 1.20V is obtained by adding these two values. The link between temperature sweep and supply frequency is shown in Figure 7.

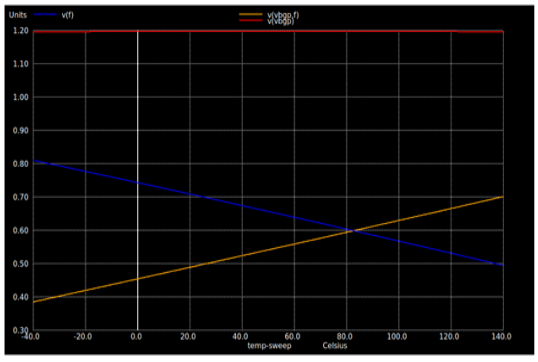

Figure 7. Temperature sweep Vs Supply frequency

4. Temperature dependence of voltage

In CTAT circuits, the output voltage has an inverse relationship with the negative TC. The output voltage of the CTAT decreases between 60 and -25V as the temperature rises. The V_{ref} was designed using the temperature

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dependence V_{CTAT}, which is depicted in Figure 8. As the threshold voltage changes more, the temperature dependency of V_{CTAT} reaches negative voltage. Regarding the temperature range of -40°C to 120°C, the voltage fluctuates between 60V and -25V. In the temperature range of 42^0C, the temperature dependency of V_{CTAT} reaches 0V. The voltage's temperature relationship is seen in Figure 8.

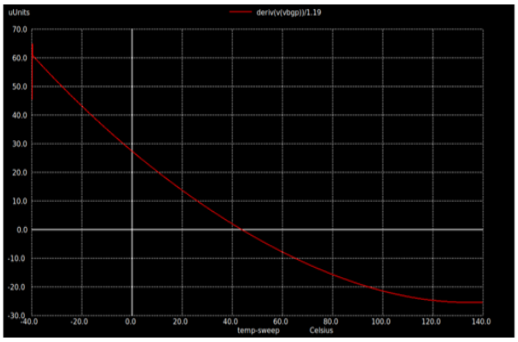

Figure 8. Characteristics of Temperature dependence of voltage

5. Supply voltage Vs sweep voltage

Depending on the source voltage, the voltage sweep signal increases linearly from minimum to maximum. With respect to the 2V sweep voltage, the bandgap VR reaches 1.11V. In relation to the sweep voltage range of 2.2V to 4V, the VR increases linearly from 1.15V to 1.22V. Figure 9 illustrates the connection between the supply voltage and sweep voltage.

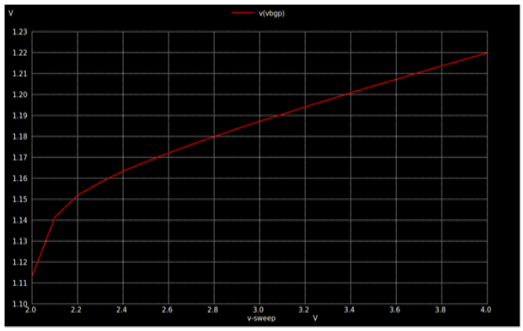

Figure 9. Characteristics of Supply voltage Vs sweep voltage

6. Temperature Dependence of Proportional Absolute Temperature Voltage

The derivative calculus, which is used to examine the rate at which electrical quantities in a circuit change, was used to study the voltage and power behaviors in the BGR circuit. The derivatives are utilized to comprehend the circuits' stability and transients. The temperature-based derivative of the PTAT voltage is calculated. Regarding the sweep voltage, the VR linearly drops from the 350–180 mV range in the temperature dependence V_{PTAT}. After that, the VR keeps the output range of 48 V steady with respect to the sweep voltage. The temperature dependence V_{PTAT} is displayed in Figure 10. The amplifier circuit analyzes power values using derivatives, which enhances the circuit's dynamic behavior and maximizes performance.

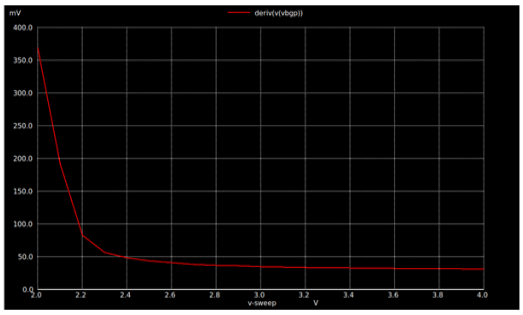

Figure 10. Characteristics of Temperature dependence of V_{PTAT}

C. Pre-layout results

The BGR circuit achieves pre-layout results for enable current, starting voltage, supply voltage, PTAT voltage, CTAT voltage, and bandgap VR, which performs better than VR to increase efficiency.

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1. Enable current

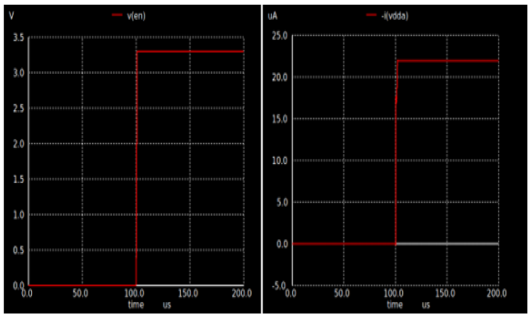

Figure 11. Enable current

To begin the current or voltage at a given time, turn on the current and voltage in the BGR circuit. The enabling voltage and current range at 100µs are 3.3V and 23µA, respectively, based on the pre-layout data. Figure 11 shows the enable current.

2. Temperature dependence of Complementary to Absolute Temperature voltage

In relation to temperature, the temperature dependence V_{CTAT} decreases linearly. The temperature dependence of V_{CTAT}, which was used to produce the V_{ref}, is depicted in the figure.

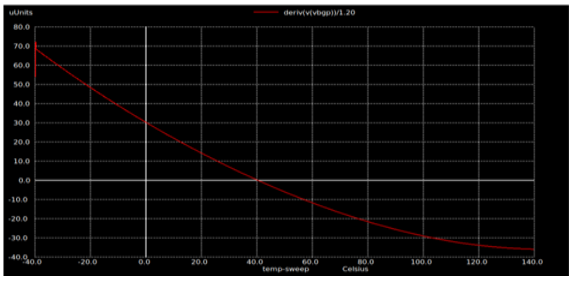

Figure 12. Characteristics of Temperature dependence of V_{CTAT}

As the threshold voltage changes more, the temperature dependency of V_{CTAT} reaches negative voltage. Regarding the temperature range of -40°C to 120°C, the voltage fluctuates between 70V and -35V. At temperatures between 40°C and 0°C, the temperature dependence of V_{CTAT} becomes 0V. The temperature dependency of V_{CTAT} is displayed in Figure 12.

3. Bandgap reference voltage based on temperature

Figure 13a shows the temperature-dependent bandgap VR. The pre-layout simulation findings take into account temperatures between -40°C and 120°C. At a particular temperature, the voltage reference reaches its maximum voltage. The VR reached a value of 1.2035V at a temperature of -40°C. 1.2066V, which is regarded as the VR's maximum level, is reached at 40°C. At temperatures between 60°C and 120°C, the VR then drops linearly with less fluctuation. In the corners, Figure 13b shows the bandgap VR.

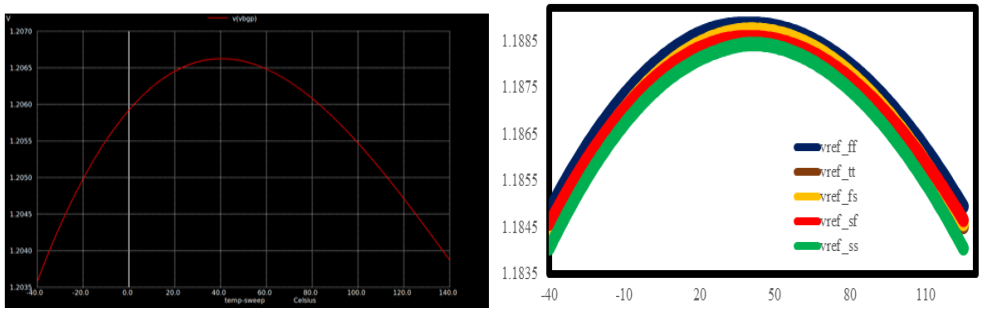

Figure 13. a) Bandgap VR based on temperature b) Bandgap VR in corners

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4. Bandgap Reference Circuit Transient Response

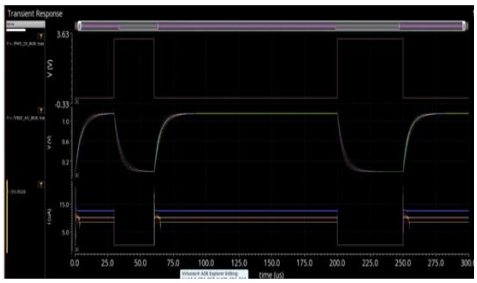

Figure 14. Characteristics of BGR transient response

Temporary alterations in the BGR circuits are caused by the external excitation in relation to time. Transient damping oscillations have an effect on the output value, which performs poorly in steady-state conditions. The short-term reactions to a stimulus are known as impulse and step responses. The transient of the BGR transient response happens between 25 and 50 µs. Following that, the reference voltage stabilizes at 1V between 75 and 200 µs. An external stimulus caused the transitory response in the BGR voltage. The effective VR values in Figure 14 indicate the BGR transient response.

D. Monte Carlo Simulation of the reference voltage

The Monte Carlo simulation for voltage reference is shown in Figure 15. Monte Carlo analysis and corner simulation are used to confirm the suggested BGR's resilience. The effects of the prediction models are explained by predicting the probability from the random variables using Monte Carlo simulation. Multiple values must be assigned in this simulation in order to average the findings and get more outcomes. The uncertain variables are changed when the uncertainty estimation problem arises. Applications in the fields of business and finance make advantage of the Monte Carlo simulation. In large projects, the simulation also determines the cost probability. Mismatch and process variables are included in the 250 Monte Carlo simulation results.

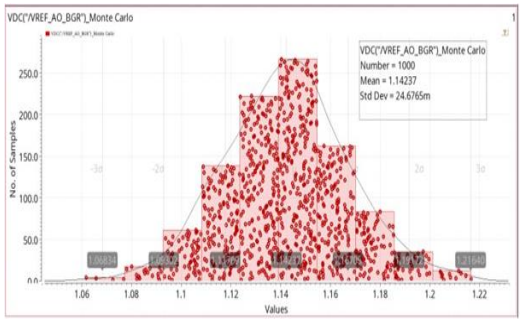

Figure 15. Monte Carlo simulation for voltage reference

The impacts of process variations and mismatches are ascertained by computing the mean and standard deviation values using this Monte Carlo simulation. The standard deviation is 24.6765, the mean value is 1.14237, and the average VR is 1.06834V. Variations in the results are introduced by the PSRR fluctuation with respect to frequency that happens in different temperature areas.

E. Loop gain and phase margin

The sum of the gains in the BGR circuits is used to compute the loop gain, which is then expressed in decibels around the feedback loop. The difference between the open and closed loop gains is known as loop gain. The negative feedback employed in the amplifier circuit is supplied by the loop gain.

The 50 dB loop gain is attained in the phase margin range up to 10^3 Hz based on the loop gain and phase margin results. The loop margin then reached 0 dB from the 10^7 Hz phase margin range. To guarantee stable operation, loop gain should be reduced within a third of the range. The phase margin is measured in degrees, with 45^0 being the safest range. Higher gains and phase margins are employed to guarantee system stability. Figure 16 shows the stability response of phase margin and loop gain.

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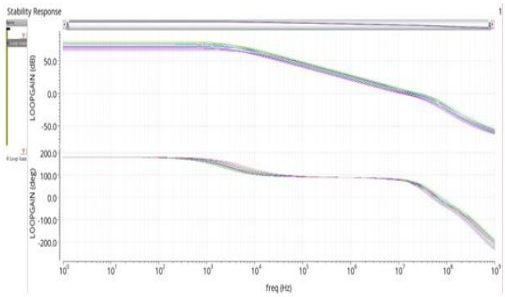

Figure 16. Characteristics of Loop gain and phase margin

F. Bandgap reference voltage mode

The corners of FF, FS, SF, SS, and TT are displayed in the BGR voltage mode, and the outcomes are achieved in the post-layout and pre-layout layouts. The corners in the post layout achieved 1.186V, 1.186V, 1.186V, 1.186V, 1.186V, and 1.186V, while the pre-layout, at a temperature range of -40^∘ C, achieved 1.186V, 1.187V, 1.187V, 1.187V, and 1.187V. The voltage reference values of 1.189V, 1.19V, 1.19V, 1.191V, and 1.19V are achieved in the post layout at 25°C, whereas the VR values of 1.19V, 1.191V, 1.191V, 1.192V, and 1.191V are obtained in the pre-layout at the same temperature.

The VRs are acquired at 125°C in both the pre-layout and post-layout. The post and pre layout PSRR values are -36.02dB. The results of the pre-layout and post-layout at various temperatures are shown in Table 1. The parts per million of the pre-layout and post-layout are shown in Table 2.

Table 1. Corner voltage values of post-layout and pre-layout with different temperatures

Corner	Vref					
	Temp= -40		***Temp= 25***		***Temp= 125***	
	Post Lay Out (V)	*Pre-layout (V)*	*Post Layout (V)*	*Pre-layout (V)*	*Post Layout (V)*	*Pre-layout (V)*
FF	1.186	1.186	1.189	1.19	1.185	1.186
FS	1.186	1.187	1.19	1.191	1.186	1.187
SF	1.186	1.187	1.19	1.191	1.186	1.187
SS	1.186	1.187	1.191	1.192	1.187	1.188
TT	1.186	1.187	1.19	1.191	1.186	1.187

Table 2. Parts Per Million units of post-layout and pre-layout

Corner	PPM	
	Post Layout (V)	*Pre-layout (V)*
FF	23.68	23.37
FS	23.47	23.12
SF	22.77	22.45
SS	23.21	23.85
TT	22.99	22.66

VII. CONCLUSION

RF front-end transceivers encounter a variety of difficulties, such as interference, signal range limitations, security requirements in wireless communication systems, and intricate design that impacts system performance. The proposed BJT is added to the PTAT generating cell to achieve a high K_I factor, and the BGR circuit is built to prevent the problems. Many transistors are used to reduce mismatches and variation effects. Aspect ratio K_A must be employed for temperature adjustment because mismatches reduced output performance and created transients in the system. The pre-layout and post-layout findings are calculated at various temperatures in this results section. The robustness of the BGR circuit, which includes mismatch and process changes in the corners, is confirmed using Monte Carlo analysis. Less fluctuation in various temperature variations is seen in PSRR data. In the post layout results, the BGR circuit produces the VR of 1.9676V at a temperature of 40^0C. The architecture of the BGR circuit will be changed in order to enhance its performance going forward.

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