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DESIGN OF 16 BIT VEDIC MULTILPLIER WITH USE OF COMPRESSOR ADDERS FOR HIGH SPEED

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ABSTRACT

With the changing world technology changes so speed is the utmost important in VLSI designs .In this paper Vedic mathematics technique 'Urdhava-triyakbhyam' is used for 16 bit multiplier in english it is called as vertically and crosswise method for multiplication and the results for each 32 bit resultant is added using compressor adders. Compressor adders actually count the no of one's and the partial products are generated parallel so the delay is less. The design is coded using VHDL and the simulation is done using ISE 12.3

Keywords: Vedic Mathematics, Urdhava-Triyakbhyam Method, Compressor Adder.

I INTRODUCTION

Vedic mathematics is derived from 'Vedas' it provides us several approach for the simplified mathematics that makes us easy to understand the complex problems. There are sixteen sutras that are enlisted below. These sutras provide not only method for calculation but also ways to think of their applications.

The sixteen sutras along there meanings are given below:

1. Anurupye Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and then adjust.
9. Puranapuranabyham – By the completion or non completion.
10. Sankalana- vyavakalanabhyam – By addition and subtraction.
11. Shesanyankena Charamena – The remainders of the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency

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The application of these sutras increases the computational skills in wide area of problems, ensuring speed and accuracy. The technique used in this paper 'urdhava-triyakbhyam' is universal method for multiplication it adds binary numbers, digits vertically and crosswise and then adds them with the help of adder.The method has been explained below for three bit digit multiplication.

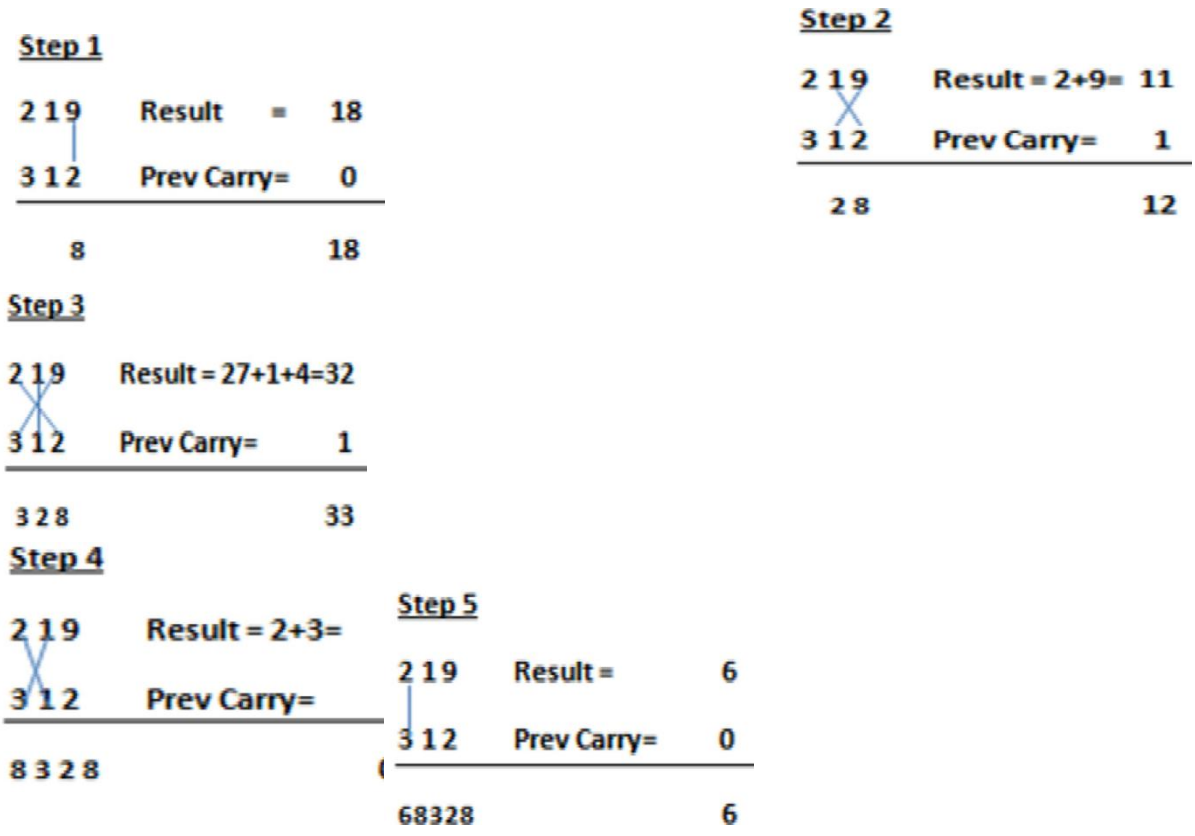

Fig.1 Steps to perform urdhava-triyakbhyam method for three bit multiplication[1]

This paper compromises of four sections. Section I describes introduction. Section II describes theory purposed and compressor adders. Section III is implementation and equations. Section IV conclusion and future scope.

1.1 Theory Purposed and Compressor Adder

The traditional designs of Vedic multiplier make use of half adder and full adders only for the partial products that cause large delay so in this paper we design a Vedic multiplier of 16 bit with use of compressor adders. The partial products are added using compressor adder. The 32 bit resulatant equations are calculated using vertically and crosswise technique.

II COMPRESSOR ADDER

It takes five inputs at a time and three bit resultant is obtained. Maximum value 101 can be obtained. The modified design of 5-3 uses three 4:1 multiplexers with this architecture we obtained lesser XOR operations and this cause improvement in speed of the multiplier. Both traditional and modified design of 5-3 is given below:

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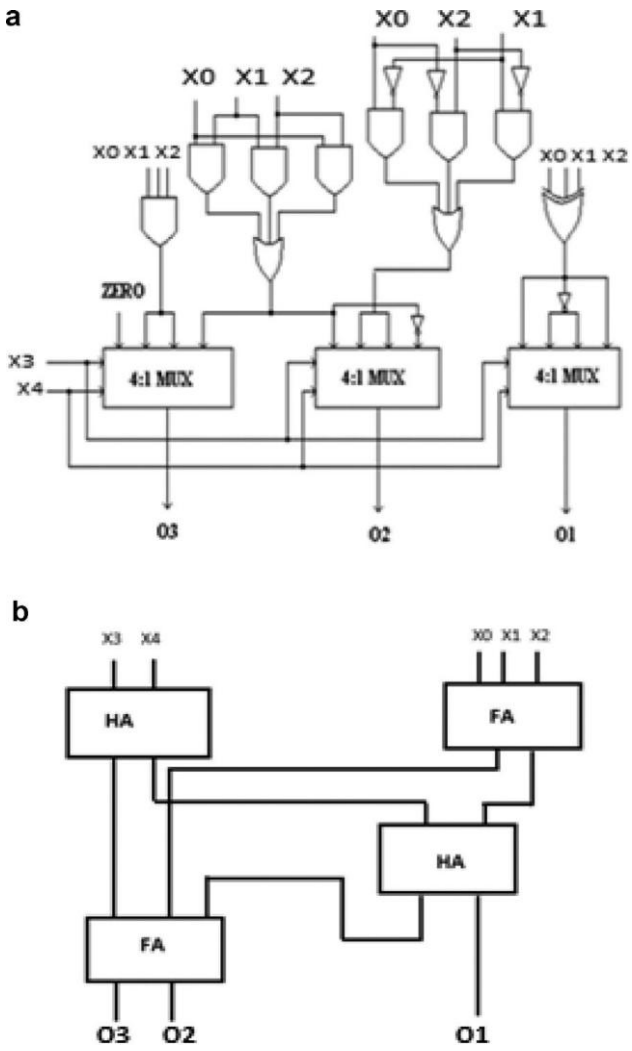

Fig.2 (a) Modified design for 5-3 compressor (b) 5-3 compressors with full adders and half-adders [1]

Compressor Adder

It takes ten input at a time and four bit resultant can be obtained and maximum of 1010 resultant can be obtained. Its circuitry consist of two 5-3 compressor adder, two full adders and a half adder.

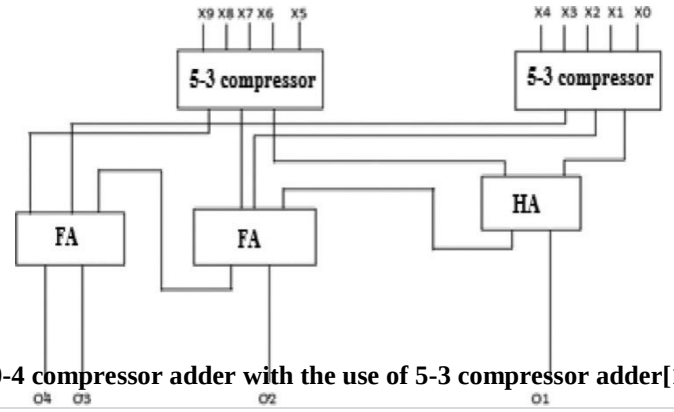

Fig.3 10-4 compressor adder with the use of 5-3 compressor adder[1]

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Compressor Adder

In this fifteen input can be taken at one time and four bit resultant can be obtained and maximum resultant can be of 1111. Its circuitry consists of two 5-3 compressor adders, five full adders and one 4 bit parallel adder. As it is using modified design of 5-3 compressor adder so delay is less.

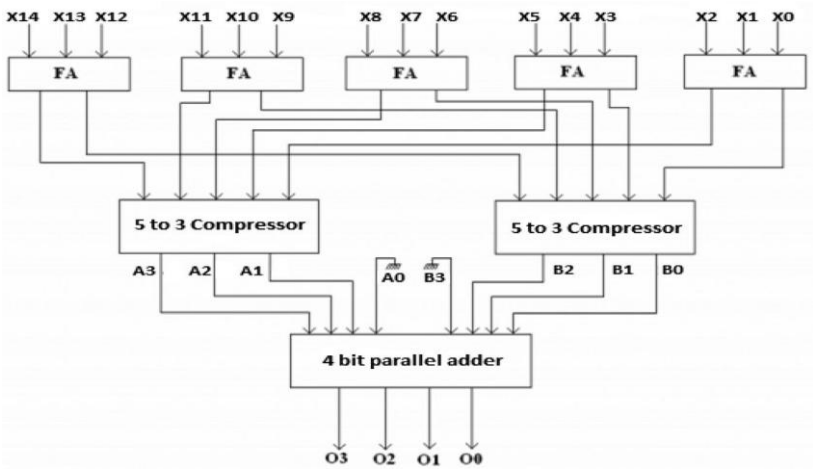

Fig.4 15-4 compressor adder with the use of 5-3 compressor adder [1]

Compressor Adder

In this twenty inputs can be taken at one time and 5 bit resultant can be obtained and maximum resultant can be obtained be of 10010. Its circuitry consists of one 15-4 compressor adder, one 5-3 compressor adder, two full adders and two half adders.

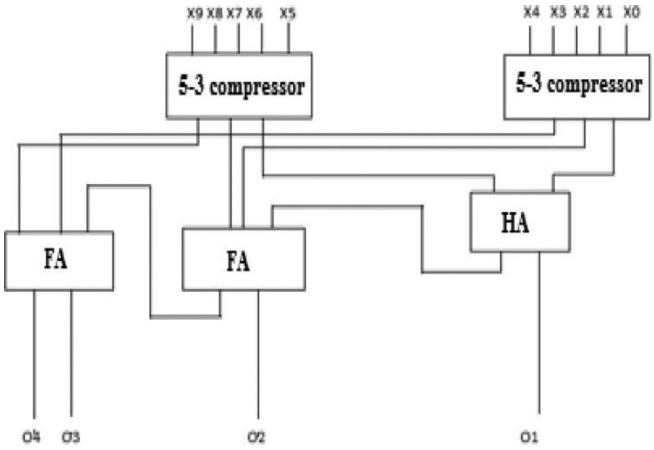

Fig.5 20-5 compressor adder with use of 15-4 and 5-3 compressor adder [1]

III IMPLEMENTATION AND EQUATIONS

3.1 Equations For 32 Bit Resultant Of 16x16 Multiplier

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As we are doing 16 x16 bit multiplication so both numbers is 16 bit long. Let both numbers be 'a' and 'b' having inputs a= $a_{16}a_{14}a_{13}a_{12}a_{11}a_{10}a_9a_8a_7a_6a_5a_4a_3a_2a_1a_0$ b= $b_{16}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$ and their product 'r' is 32 bit i.e. (r_{31-0}) and carry signal will be $c_1 - c_{89}$

Equations that are going to be implemented are as follow:

$S_0 = a_0b_0$

$C_1S_1 = a_0b_1 + a_1b_0$

$C_3C_2S_2 = C_1 + a_0b_2 + a_2b_0$

$C_5C_4S_3 = C_2 + a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0$

$C_7C_6S_4 = C_4 + C_3 + a_0b_4 + a_1b_3 + a_2b_2 + a_3b_1 + a_4b_0$

$C_{10}C_9C_8S_5 = C_6 + C_5 + a_0b_5 + a_1b_4 + a_2b_3 + a_3b_2 + a_4b_1 + a_5b_0$

$C_{13}C_{12}C_{11}S_6 = C_8 + C_7 + a_0b_6 + a_1b_5 + a_2b_4 + a_3b_3 + a_4b_2 + a_5b_1 + a_6b_0$

$C_{16}C_{15}C_{14}S_7 = C_{11} + C_9 + a_0b_7 + a_1b_6 + a_2b_5 + a_3b_4 + a_4b_3 + a_5b_2 + a_6b_1 + a_7b_0$

$C_{19}C_{18}C_{17}S_8 = C_{10} + C_{12} + C_{14} + a_0b_8 + a_1b_7 + a_2b_6 + a_3b_5 + a_4b_4 + a_5b_3 + a_6b_2 + a_7b_1 + a_8b_0$

$C_{22}C_{21}C_{20}S_9 = C_{17} + C_{15} + C_{13} + a_0b_9 + a_1b_8 + a_2b_7 + a_3b_6 + a_4b_5 + a_5b_4 + a_6b_3 + a_7b_2 + a_8b_1 + a_9b_0$

$C_{25}C_{24}C_{23}S_{10} = C_{20} + C_{18} + C_{16} + a_0b_{10} + a_1b_9 + a_2b_8 + a_3b_7 + a_4b_6 + a_5b_5 + a_6b_4 + a_7b_3 + a_8b_2 + a_9b_1 + a_{10}b_0$

$C_{28}C_{27}C_{26}S_{11} = C_{23} + C_{21} + C_{19} + a_0b_{11} + a_1b_{10} + a_2b_9 + a_3b_8 + a_4b_7 + a_5b_6 + a_6b_5 + a_7b_4 + a_8b_3 +$

$a_9b_2 + a_{10}b_1 + a_{11}b_0$

$C_{32}C_{31}C_{30}C_{29}S_{12} = C_{26} + C_{24} + C_{22} + a_0b_{12} + a_1b_{11} + a_2b_{10} + a_3b_9 + a_4b_8 + a_5b_7 + a_6b_6 + a_7b_5 + a_8b_4 +$

$a_9b_3 + a_{10}b_2 + a_{11}b_1 + a_{12}b_0$

$C_{36}C_{35}C_{34}C_{33}S_{13} = C_{29} + C_{27} + C_{25} + a_0b_{13} + a_1b_{12} + a_2b_{11} + a_3b_{10} + a_4b_9 + a_5b_8 + a_6b_7 +$
$a_7b_6 + a_8b_5 + a_9b_4 + a_{10}b_3 + a_{11}b_2 + a_{12}b_1 + a_{13}b_0$

$C_{40}C_{39}C_{38}C_{37}S_{14} = C_{33} + C_{30} + C_{28} + a_0b_{14} + a_1b_{13} + a_2b_{12} + a_3b_{11} + a_4b_{10} + a_5b_9 + a_6b_8 +$
$a_7b_7 + a_8b_6 + a_9b_5 + a_{10}b_4 + a_{11}b_3 + a_{12}b_2 + a_{13}b_1 + a_{11}b_0$

$C_{44}C_{43}C_{42}C_{41}S_{15} = C_{37} + C_{34} + C_{31} + a_0b_{15} + a_1b_{14} + a_2b_{13} + a_3b_{12} + a_4b_{11} + a_5b_{10} + a_6b_9 +$

$a_7b_8 + a_8b_7 + a_9b_6 + a_{10}b_5 + a_{11}b_4 + a_{12}b_3 + a_{13}b_2 + a_{14}b_1 + a_{15}b_0$

$C_{48}C_{47}C_{46}C_{45}S_{16} = C_{32} + C_{35} + C_{33} + a_0b_{15} + a_1b_{14} + a_2b_{13} + a_3b_{12} + a_4b_{11} + a_5b_{10} + a_6b_9 +$
$a_7b_8 + a_8b_7 + a_9b_6 + a_{10}b_5 + a_{11}b_4 + a_{12}b_3 + a_{13}b_2 + a_{14}b_1 + a_{15}b_0$

$C_{52}C_{51}C_{50}C_{49}S_{17} = C_{45} + C_{42} + C_{39} + C_{36} + a_2b_{15} + a_3b_{14} + a_4b_{13} + a_5b_{12} + a_6b_{11} + a_7b_{10} + a_8b_9 +$
a_9b_8
$+ a_{10}b_7 + a_{11}b_6 + a_{12}b_5 + a_{13}b_4 + a_{14}b_3 + a_{15}b_2$

$C_{56}C_{55}C_{54}C_{53}S_{18} = C_{49} + C_{43} + C_{46} + C_{40} + a_3b_{15} + a_4b_{14} + a_5b_{13} + a_6b_{12} + a_7b_{11} + a_8b_{10} + a_9b_9 +$
$a_{10}b_8$
$+ a_{11}b_7 + a_{12}b_6 + a_{13}b_5 + a_{14}b_4 + a_{15}b_3$

$C_{60}C_{59}C_{58}C_{57}S_{19} = C_{53} + C_{50} + C_{47} + C_{44} + a_4b_{15} + a_5b_{14} + a_6b_{13} + a_7b_{12} + a_8b_{11} + a_9b_{10} + a_{10}b_9$
$+ a_{11}b_8 + a_{12}b_7 + a_{13}b_6 + a_{14}b_5 + a_{15}b_4$

$C_{63}C_{62}C_{61}S_{20} = C_{57} + C_{54} + C_{51} + C_{48} + a_5b_{15} + a_6b_{14} + a_7b_{13} + a_8b_{12} + a_9b_{11} + a_{10}b_{10} + a_{11}b_9 +$
$a_{12}b_8$
$+ a_{13}b_7 + a_{14}b_6 + a_{15}b_5$

$C_{66}C_{65}C_{64}S_{21} = C_{61} + C_{58} + C_{55} + C_{45} + a_6b_{15} + a_7b_{14} + a_8b_{13} + a_9b_{12} + a_{10}b_{11} + a_{11}b_{10} + a_{12}b_9 +$
$a_{13}b_8 + a_{14}b_7 + a_{15}b_6$

$C_{69}C_{68}C_{67}S_{22} = C_{56} + C_{59} + C_{62} + C_{64} + a_6b_{15} + a_7b_{14} + a_8b_{13} + a_9b_{12} + a_{10}b_{11} + a_{11}b_{10} + a_{12}b_9 +$
$a_{13}b_8 + a_{14}b_7 + a_{15}b_6$

$C_{72}C_{71}C_{70}S_{23} = C_{67} + C_{65} + C_{63} + C_{60} + a_8b_{15} + a_9b_{14} + a_{10}b_{13} + a_{11}b_{12} + a_{12}b_{11} + a_{13}b_{10} +$
$a_{14}b_9 + a_{15}b_8$

$C_{75}C_{74}C_{73}S_{24} = C_{70} + C_{68} + C_{66} + a_9b_{15} + a_{10}b_{14} + a_{11}b_{13} + a_{12}b_{12} + a_{13}b_{11} + a_{14}b_{10} + a_{15}b_9$

$C_{78}C_{77}C_{76}S_{25} = C_{70} + C_{68} + C_{66} + a_{10}b_{15} + a_{11}b_{14} + a_{12}b_{13} + a_{13}b_{12} + a_{14}b_{11} + a_{15}b_{10}$

$C_{81}C_{80}C_{79}S_{26} = C_{76} + C_{76} + C_{72} + a_{11}b_{15} + a_{12}b_{14} + a_{13}b_{13} + a_{14}b_{12} + a_{15}b_{11}$

$C_{32}C_{33}S_{27} = C_{79} + C_{77} + C_{75} + a_{12}b_{15} + a_{13}b_{14} + a_{14}b_{13} + a_{15}b_{12}$

$C_{85}C_{84}S_{28} = C_{82} + C_{80} + C_{78} + a_{13}b_{15} + a_{14}b_{14} + a_{15}b_{13}$

$C_{87}C_{86}S_{29} = C_{84} + C_{83} + C_{81} + a_{14}b_{15} + a_{15}b_{14}$

$C_{88}S_{30} = C_{85} + C_{86} + a_{15}b_{15}$

$C_{89}S_{31} = C_{88} + C_{87}$

As for these equations we require adders which can add 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19 bits at same time so the compressor adders come into play. The structure of compressor adders has been given below we have used 5-3, 10-4, 15-4 and 20-5 compressor adder.

IV CONCLUSION AND FUTURESCOPE

In this paper the Vedic multipliers design is made with use of vertically and crosswise technique with compressor adders as with the use of multiplexers circuitry in compressor adders results in less delay count and speed increases so the proposed theory or architecture can be used in where there are stringent demands of area, speed and power. We can compare speed with various other multipliers like booth multipliers, Wallace tree and array multipliers which uses traditional adders which clearly shows better performance of modified Vedic multiplier. It can also be used in various digital signal processing designs.

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