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AN EFFICIENT IMPLEMENTATION OF PULSE SHAPING FIR FILTER FOR MULTISTANDARD DDC

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ABSTRACT

In several DSP applications speed is vital particularly for the initial process of the information, when that there's reduced rate and becomes a lot of appropriate. The Digital Down Conversion could be a planned technique that has the lead role during a band restricted high sample rate digitized signal, lower frequency mixer and reduced sample rate whereas holding all the knowledge. The PFIR provides a further down-sampling issue to cut back the CIC filter necessities and provides channel property per the adjacent channel interference and interference characteristics. Pulse shaping FIR digital filters is understood that for avoiding intersymbol interference (ISI), sure time-domain constraints for planning best pulse shaping filters ought to be thought of. Its operate is to translate a passband signal comprising one or a lot of radio or intermediate frequency (RF or IF) carriers to at least one or a lot of baseband channels for reception and devastation. The rectifier has some influence on the general rate modification of the filter chain, because it could need associate degree over-sampled image input, for temporal order recovery for example. the whole system is synthesized and simulated victimisation Xilinx's Spartan 6's 6SLX45CSG324-3

Keywords: DDC, Distributed Arithmetic, FIR, Pulse Shaping(PFIR),VLSI

I. INTRODUCTION

A basic part of several communications systems is Digital Down Conversion (DDC) and is the part of SDR. SDR can act as a key enabling technology for a variety of other reconfigurable radio equipments commonly discussed in the advanced wireless market. While SDR is not required to implement any of these radio types, SDR technologies can provide these types of radio with the flexibility necessary for them to achieve their full potential, the benefits of which can help to reduce cost and increase system efficiency. In fashionable knowledge transmission systems, bits or teams of bits (symbols) ar usually transmitted within the kind of individual pulses of energy. an oblong pulse is perhaps the foremost basic. it's simple to implement in an exceedingly real-world system as a result of it will be directly compared to gap and shutting a switch, that is substitutable with the conception of binary data. for instance, a "1" bit may be accustomed activate AN energy supply for the period of 1 pulse interval (τ seconds), which might manufacture AN output level, "A". Alternately, a "0" bit would close up the energy supply, manufacturing AN output level of zero throughout one pulse interval. Communications systems usually rely on the relationships between multiple carriers. These

carriers could also be an equivalent frequency however with completely different|completely different} phase; or they will be utterly different frequencies. In either case, troubling the part relationships would be a nasty issue. For this reason, most DDC designers can attempt to use linear part filters solely. These seem as an easy delay to the signal, and as all components of the signal ar delayed by an equivalent quantity, the signal's integrity is preserved. In our description, we have a tendency to delineate devastation as merely "throwing away" samples. this is often a legitimate issue to try to to for number changes within the sampling rate; for instance, once decimating a information measure restricted signal

II. LITERATURE SURVEY

[1] This paper proposes economical constant multiplier factor design supported vertical-horizontal binary common sub-expression elimination (VHBCSE) algorithm for planning a reconfigurable finite impulse response (FIR) filter whose coefficients will dynamically modification in real time. The 2-bit BCSE has been applied vertically across adjacent constants on the 2-D house of the coefficient matrix ab initio, followed by applying variable-bit BCSE rule horizontally among every constant. Power delay product (PDP) for the VHBCSE algorithms are achieved over those of the sooner multiple constant multiplication (MCM) algorithms for economical fastened purpose reconfigurable FIR filter synthesis.

[2] A memory based mostly} upsampling/interpolating FIR filter modification/extension to distributed arithmetic (DA) based FIR filters is planned that may be used for any filter coefficients set. The signal process is performed exploitation FPGAs since multipliers square measure scarce/expensive resources among FPGAs whereas registers and such square measure ample. Upsampling a digital stream is sometimes performed by inserting zeros between original samples followed by a coffee pass filter to reject pictures. Compared to basic prosecuting attorney primarily based filter styles wherever partial products/sums square measure hold on in memory blocks. These samples square measure output consecutive employing a straight counter, eliminating zero insertions and saving circuit components.

[3] Digital filters square measure necessary in digital transmitter / receiver aspect and recognition of code outlined Radio (SDR) is forcing complicated digital signal process blocks to be enforced in parallel style flow on FPGA. The goal of this paper is to develop economical pipelined poly-phase FIR filter structures in VHDL language for RTL synthesis on FPGA. The planned structures contain absolutely parallel poly-phase devastation and interpolation FIR filter models. The formulation of distributed arithmetic technique with poly-phase decomposition, that represents the core of designed models and it describes mentioned poly-phase FIR VHDL models. The intensive stress are placed on economical pipelined implementation with glorious registered performance and best style size balance conjointly it deals with fast style and simulation of planned VHDL models. The results of RTL synthesis is finally mentioned

[4] A multi-mode reconfigurable digital intermediate frequency (IF) module for code outlined radio (SDR) transmitters is bestowed. It supports variable input sample rate from seven kilocycle per second to thirty.72 MHz, and variable signal information measure from five kilocycle per second to 20MHz. Its output sample rate is eighty megahertz or one hundred sixty megahertz The digital IF module consists of seven half-band filters, a digital up convertor (DUC) and four FIR filters. every stage are often turned off singly. The 10-bit signal to

noise and distortion magnitude relation (SNDR) is higher than fifty four.5dB, whereas the 12-bit input SNDR is 60dB.This digital IF module supports each ancient narrowband industry-specific network and LTE (Long Term Evolution) cluster communication applications.

[5] This paper proposes a changed reconfigurable design for finite impulse response (FIR) filter. The planned design uses shift and add unit together with changed process component (MPE) unit. MPE units and structural adders square measure enforced with 4:2 compressors, that improve the performance of FIR filter. The planned filter is enforced exploitation gate level Verilog lipoprotein and synthesized exploitation Xilinx's Spartan 6's 6slx45csg324-3. The synthesis results square measure compared with recently printed architectures and show a major improvement in space, power and delay.

III. EXISTING SYSTEM

In existing system a two-step optimization technique was used for designing a reconfigurable VLSI architecture of an interpolation filter for multistandard digital up converter (DUC) to reduce the power and area consumption They initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multistandard DUC for three different standards. In the next step, a 2-bit binary common sub expression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multistandard DUC.

IV. PROPOSED SYSTEM

In proposed system we used pulse shaping FIR decimation filter operation.An ADC samples the detected analog signal and feeds into the DDC processing chain. Optionally, in advanced systems, an initial frequency translation (to shift the center frequency from pass band to baseband), RF processing (for example, channel estimation and carrier recovery), and additional filtering (decimation) can be performed prior to the base down-conversion function. A mixer is used in combination with a vector of one or more sinusoids to channelize the signal, then each channel is filtered (to provide decimation and channel selectivity), and finally demodulated (or otherwise interpreted). This application note covers the functions of the main mixer and filters (indicated by the red box in the diagram), with some reference to converters and demodulators. The optional functions are discussed briefly where relevant to provide some system context. Transmitting a signal at high modulation rate through a band-limited channel can create intersymbol interference. As the modulation rate increases, the signal's bandwidth increases. When the signal's bandwidth becomes larger than the channel bandwidth, the channel starts to introduce distortion to the signal. This distortion usually manifests itself as intersymbol interference. Not every filter can be used as a pulse shaping filter..

4.1 System Overview

A Digital Down Converter (DDC) is the counterpart component to the DUC and is, therefore, equally important as a component in the same application systems. Its function is to translate a pass band signal comprising one or more radio or intermediate frequency (RF or IF) carriers to one or more baseband channels for demodulation and interpretation

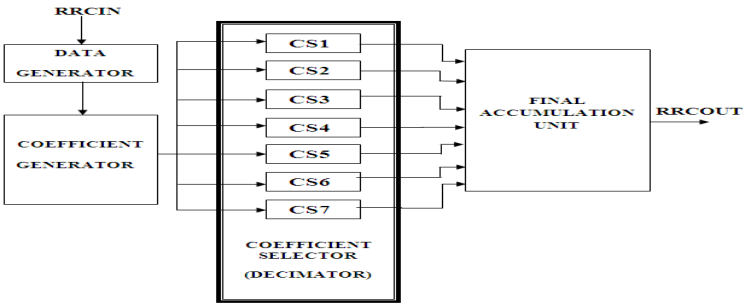

Fig 1: Block Diagram of Proposed System

It achieves this by performing: mixing to shift the signal spectrum from the selected carrier frequencies to baseband, decimation to reduce the sample rate, and filtering to remove adjacent channels, minimize aliasing, and maximize the received signal-to-noise ratio (SNR). The DDC input signal has a relatively high sample rate, generally, the output sample rate of an Analog-to-Digital Converter (ADC) which samples the detected signal (often after analog frequency translation and pre-processing), while the output is a much lower rate, for example, the symbol rate of a digital communications system for demodulation002E

4.2 Overall Block Diagram

The figure 2 shows the overall block diagram, let us discuss each module in detail based on the transmission conditions.

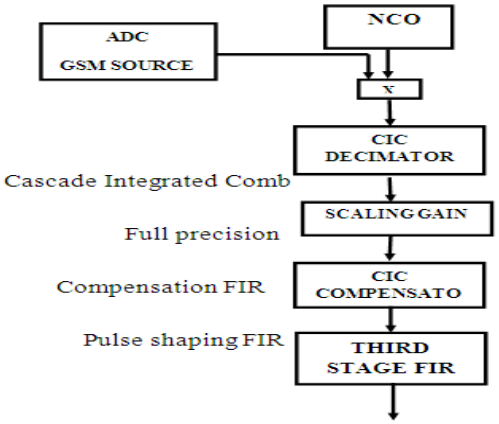

Figure 2 Block Diagram for Digital Down Converter

4.3 Data Generator

When the clock signal is applied to the data generator, the data has been mechanically furnished by sampling the input signal. The input data is sampled based on the selected value of the selection lines of multiplexer. Figure 3

shows the flow diagram representation of the DG block. It is used to sample the input data (RRCIN) depending on the selected value of the decimation factor selection parameter (INTP_SEL).

4.4 Coefficient Generator

The CG block performs the multiplication between the inputs and the filter coefficients. The data flow diagram of the CG block for programmable coefficient sets is shown in Figure 3. The steps mentioned in the previous section have been adopted to enable low area consumption and low complexity. Coefficient generator comprises of first coding pass, second coding pass, Partial Product Generator, multiplexer unit and addition.

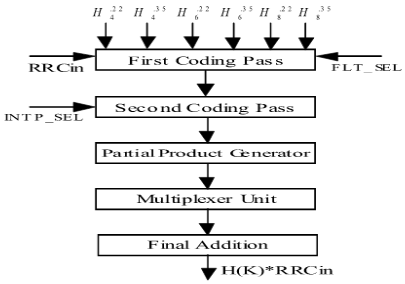

Figure 3 Data Flow Diagram of CG Block

Functionality of each block shown in Figure 4 is described as follows.

The First Coding Pass takes the input from the output produced by the data generator. The inputs are selected from the data generator are processed and the outputs are produced based on the selected values of the selection lines of multiplexer. The Architecture of FCP block is shown in Figure 4

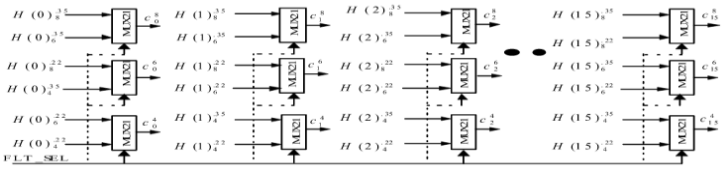

Figure 4 Architecture of FCP Block

The operation of the second coding pass is similar to the first coding pass. It takes the input from the produced output by second coding pass. It produced the output based on the inputs selection which are processing then based on the selected values of the selection lines of the multiplexer, the output has been produced. The Architecture of SCP block is shown in Figure 3

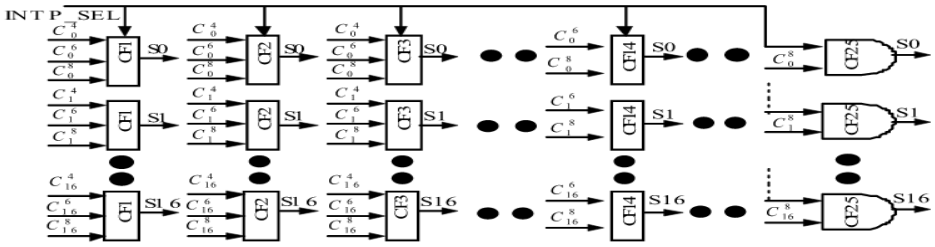

Figure 5 Architecture of SCP Block

Carry save adder is used to generate the partial products. While using this method, the steps of addition are reduced as three to two. So that delay can be reduced and the speed has been increased. The Architecture of PPG block is shown in Figure 6

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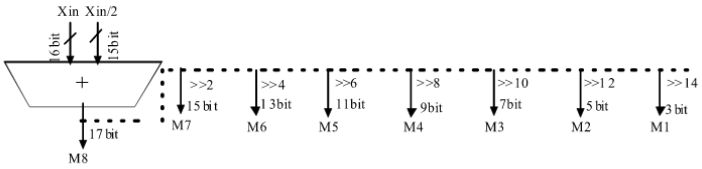

Figure 6 Architecture for Implementation of PPG Block

4.5 Coefficient Selector

The Coefficient Selector takes the input from the output of the coefficient generator which selects the required data for processing. Then the selected inputs are simulated in AND logic to perform multiplication operation. The Hardware architecture of CS block is shown in Figure 7

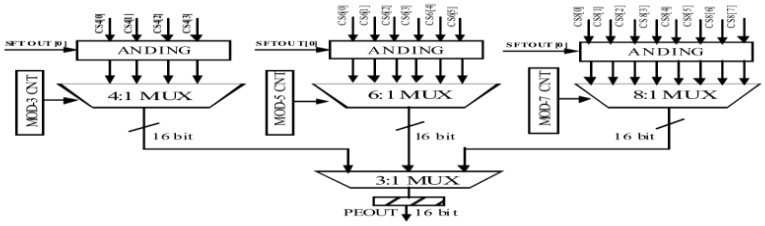

Figure 7 Architecture for Implementation of PPG Block

4.6 Final Accumulation Unit

The inputs for accumulation were taken from the output of the data generator, coefficient generator and coefficient selector which are then added and the filter output will be produced. Depending on the coded coefficients, the multiplexer unit will select the appropriate data generated from the PPG unit. The Hardware architecture of FA block is shown in Figure 8

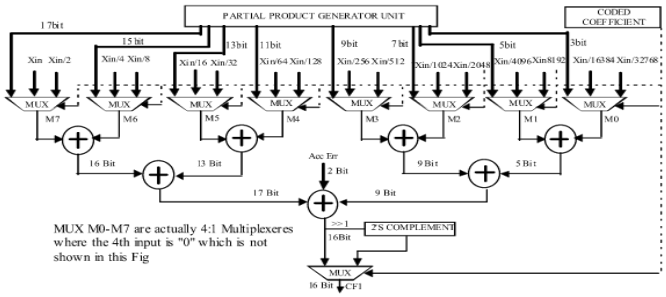

Figure 8 Hardware Architecture of FA Block

4.7 Distributed Arithmatic Algorithm

Distributed arithmetic (DA) is an efficient multiplication-free technique for calculating inner products. The multiplication operation is replaced by a mechanism that generates partial products and then sums the products together. The key difference between distributed arithmetic and standard multiplication is in the way the partial products are generated and added together.The ability of distributed arithmetic to reduce a multiply operation into a series of shifts and additions yields great potential for implementing various DSP systems at a significantly reduced area. However, this reduction in area comes at the cost of increased power and decreased

throughput. This trade-o among area, throughput, and power has generated substantial research into making DA-based designs a more viable alternative to the standard multiply-accumulate designs for certain applications.

V. RESULTS AND DISCUSSION

Synthesized speech can be created by concatenating pieces of recorded speech that are stored. Systems differ in the size of the stored speech units. The quality of a speech synthesizer is judged by its similarity to the human voice and by its ability to be understood clearly

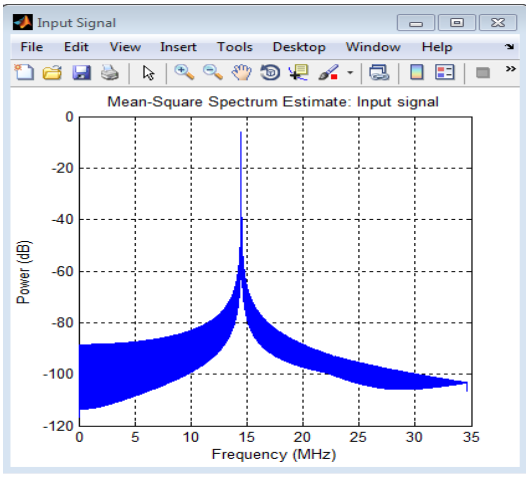

Fig 9 Input Signal

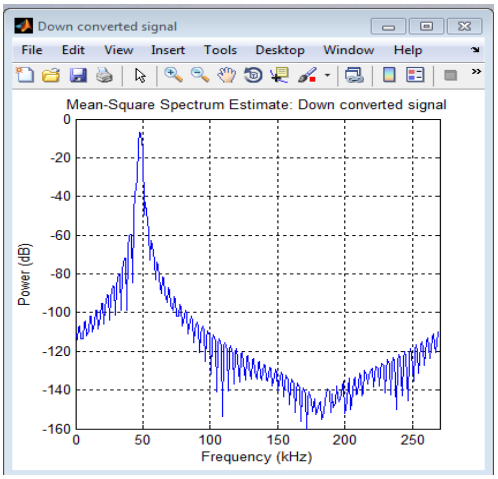

Fig 10 Output Signal

Table 1 Comparison Results on FPGA Platform

References		Method Used	Filter Length	Max.Freq.	Slices	Gate count
Existing	XC2VP4	2 Bit BCSE	25/37/49/ TAP 16X17	83.4	3142	29470
	XCV2000E			49.5	1788	30564
	XCV3000			58.9	1742	29425
	XC3S400N			69.74	1749	29545
XCV2000E		DA Based	64 TAP 8X8	64	1031	23878

VI. CONCLUSION

This brief addresses the pulse shaping FIR filter for coming up with the reconfigurable filter used in multistandard DDC, that is a crucial part of SDR/cognitive radio. This transient conjointly offers solutions to the issues to build the desired filter a lot of economical by reducing space and power together with improvement within the most in operation frequency of the style. Comparisons of results of the planned design with alternative out there reconfigurable FIR filter designs enforced on FPGA similarly as ASIC platform demonstrate deserves of the planned architecture in terms of speed, power, and space consumption.

The planned style appears to be remarkably appropriate for next generation multistandard reconfigurable DDC of SDR system wherever power and space ought to be optimized. The completed styles square measure economical each in terms of resources and of power, taking advantage of the advanced options of Xilinx devices and also the high performance of its DSP science core. In Future, the Cascaded Integrated Comb filter, Compensation FIR filter square measure designed and also the CIC compensation filter (CFIR) is associate degree interpolating low-pass FIR filter. It provides an extra increase in sample rate, reducing the necessities on the CIC and limiting the amount of stages needed, whereas conjointly providing moderate passband filtering of the GMSK modulated signal (although this demand is a smaller amount tight wherever smart} GMSK modulator with good pulse-shaping properties has been used). a crucial further perform provided by the CFIR is compensation for the passband droop introduced by the CIC filter.

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