A CONTROL METHOD FOR BUCK-BOOST VOLTAGES USING MULTILEVEL INVERTERS FOR APPLICATION OF HYBRID ELECTRIC VEHICLE

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ABSTRACT

This paper proposes a closed loop control an implemented to an achieve a smooth speed control irrespective of the variations in the load and input voltage fluctuations, using The space vector pulse width amplitude modulation (SVPWAM) is an efficient control technique which increases the power density and increases the efficiency. When an inverter fed with proportional and integral (PI) control technique is used for the control of dynamic load conditions, it gives a better speed and torque control. The study analysis includes the buck boost operation of the input DC of the inverter to have a control as per the load variations, Also an attempt to reduce the THD has been made by using the closed loop control has examined by simulation/MATLAB

Keywords- Buck Bust Voltages, Hybrid Electric Vehicles, PI-Control, THD, Space Vector Pulse Width Amplitude Modulation.

I. INTERODCTION

An adjustable speed drive (ASD) is a device used to provide continuous range process speed control (as compared to discrete speed control as in gearboxes or multi-speed motors). An ASD is capable of adjusting both speed and torque from an induction or synchronous motor. An electric ASD is an electrical system used to control motor speed. Adjustable speed drives are the most efficient types of drives[8]-[10]. They are used to control the speeds of both AC and DC motors. The most widely used PWM schemes for three-phase voltage source inverters are carrier-based sinusoidal PWM and space vector PWM (SVPWM). There is an increasing trend of using space vector PWM (SVPWM) because of their easier digital realization and better dc bus utilization. Currently, two existing inverter boogies are used for Hybrid electric vehicles the conventional threephase inverter with a high voltage battery and a three-phase pulse width modulation (PWM) Inverter with a dc/dc boost front end. The conventional PWM Inverter imposes high stress on switching devices and motor thus limits the motor's constant power speed range (CPSR), which can be alleviated through the dc-dc boosted PWM inverter The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor's constant power speed range (CPSR), which can be alleviated through the dc-dc boosted PWM inverter [1]. The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the

motor stator. The inverter switching action is being controlled by the basic PWM techniques by which the performance of the inverter is poor as THD content in its output is more accompanied by the switching losses and reduced efficiency. In this paper, space vector pulse width modulation was proposed to overcome these defects. This improves the efficiency of the inverter and when fed to a machine it gives better control of speed and torque characteristics[8]. This paper proposes a simple control method for buck-boot voltages using cascade multilevel inverters for hybrid electric vehicles, a closed loop control with a PI controller to further improve the efficiency.

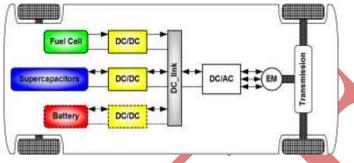
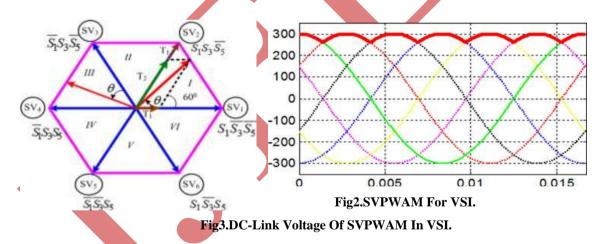


Fig.1 Electric Vehicles Drive System

II. SVPWAM FOR VSI

2.1 Principle of SVPWAM Control in VSI



The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors[6][7]. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore, S1 and S2 keep constant ON, and S3 and S6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage V_{ac} at this time. Consequently, the dc-link voltage should present $a6\omega$ varied Feature to maintain a desired output voltage. The corresponding waveform is shown in solid line in Fig3. A dc-dc conversion is needed in the front stage to generate this 6ω voltage. The original equations for time period T_1 and T_2 are [1]

$$T1 = \frac{\sqrt{3}}{2} m \sin\left(\frac{\pi}{3} - \theta\right); \quad T2 = \frac{\sqrt{3}}{2} m \sin\left(\theta\right); \dots (1)$$

Where $\theta \in [0, \pi/3]$ is relative angle from the output voltage Vector to the first adjacent basic voltage vector like in Fig.2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics. Therefore, in order to keep the switching period constant but still keep the same pulse width as the original one, the new time periods can be calculated as[1]

$$T1'/Ts = T1/(T1+T2)....(2)$$

2.2 Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within $[-60^{\circ}, 60^{\circ}]$, at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage V_{dc} , and the current stress is equal to output current i_a . Thus the switching loss for each switch is [1]

$$P_{\text{sw-I}} = \frac{2 - \sqrt{3}}{\pi} \cdot \frac{\text{Im V } dc}{\text{V ref Iref}} \cdot \text{E S R . f sw}$$
 (3) where ESR, Vref, Iref are the references.

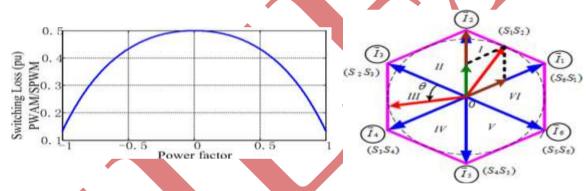


Fig.4 (Svpwampower Loss/SPWM Power Loss) Versus
Power Factor In VSI

Fig5.Conventional CSI And Its Corresponding SVPWAM

Since the SVPWAM only has PWM switching in two 60° sections, the integration over 2π can be narrowed down into integration within two 60°. PSW-I = $(2\sqrt{3})/\pi$. (ImVDC/(Vref Iref) .ESR .fsw(4) The switching loss for a conventional SPWM method is[1] PSW -I'= $(2/\pi)$.(ImVDC/(Vref Iref) .ESR.fsw(5)

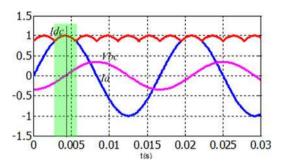
In result, the switching loss of SVPWAM over SPWM is f = 13.4%. However, when the power factor decreases, the switchingloss reduction amount decreases because the switching current increases as Fig 4. shows. As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50-87%.

III. SVPWAM FOR CSI

3.1 Principle of SVPWAM in CSI

The principle of SVPWAM in CSI is also to eliminate the zero vectors. As shown in Fig5. for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower

phase legs are conducting together at any moment[2]. Thus, for each switch, it only needs to do PWM switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vectors selected in each sector, this method brings down the switching frequency by one-third.



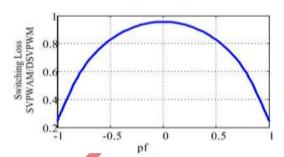


Fig6.Switching Voltage And Current When Pf = 1.

Fig 7. Sypwampower Loss/SPWM Power Loss Versus Power Factor In VSI.

Similarly, the dc-link current in this case is a 6ω varied current. It is the maximum envelope of six output currents:

Ia, Ib, Ic,—Ia,—Ib,—Ic, as shown in Fig 6. For example, in sector I, S1 always keeps ON, so the dc-link current is equal to Ia. The difference between dc-link current in CSI and dc-link voltage in VSI is dc-link current in CSI is overlapped with the phase current, but dc-link voltage in VSI is overlapped with the line voltage, not the phase voltage[2]. The time intervals for two adjacent vectors can be calculated in the same way as equation (1) and (2).

3.2 Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dc link current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig 6. Thus, the switching loss for a single switch is determined by [1] $P_{SW-CSI} = (2-\sqrt{3})/\pi$ (idc V1-lpeak)/Vref Iref . E_{SR} fsw.....(6)

When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result in equation (6). The corresponding switching loss ratio between SVPWAM and discontinuous SVPWM is shown in Fig 7.

IV. TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc-dc conversion which converts a dc voltage or current into a 6ω varied dc-link voltage or current; VSI or CSI for which SVPWAM is applied[8]. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter [1]. The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current Ipn to have a constant average value, the open zero state duty cycle Dop will be regulated instantaneously to control Ipm to have a 6ω fluctuate average value, resulting in a pulse type 6ω waveform at the real dc-link current Ipn, since I_1 is related to the input dc current Iin by a transfer function[1]

$$I1 = [(1 - Dop) / (1 - 2Dop)] Iin....(7)$$

V. CASE STUDY: 1-KWBOOST-CONVERTER INVERTER FOR EV MOTOR DRIVE APPLICATION

1. Basic Control Principle

2. The circuit schematic and control system for a 1-kW boost converter inverter motor drive system is shown in Fig. 8. A 6ω dc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for t he system are input voltage is 100–200 V; the average dc-linkvoltage is 300 V; output line-to-line voltage rms is 230 V; and frequency is from 60 Hz to 1 kHz.

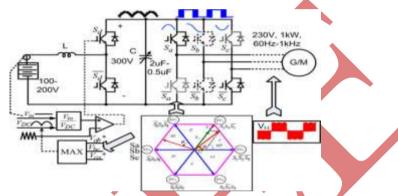


Fig 8. SVPWAM-Based Boost-Converter-Inverter Motor Drive System

3. Voltage Constraint and Operation Region

The constraint is determined by the minimum point of the 6ω Dc-link voltage. Beyond this region, conventional SPWM can be implemented. However, the dc-link voltage in this case still varies with 6ω because of the small film capacitor we selected. Thus, a modified SPWM with varying dc-link voltage will be adopted during the motor start up as shown in Fig 8. Hence, the system will achieve optimum efficiency when the motor is operating a little below or around nominal voltage. When the motor demands a low voltage during start up, efficiency is the same as the conventional SPWM-controlled inverter.

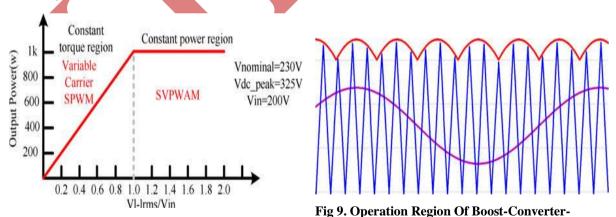


Fig 10. Variable Carrier SPWM Control In

Inverter EV Traction Drive

Buck Mode

In SVPWAM control of boost mode, dc-link voltage varies with the output voltage, in which the modulation index is always kept maximum[2]. So, when dc-link voltage is above the battery voltage, dc-link voltage level varies with the output voltage. The voltage utilization increased and the total power stress on the devices has been reduced[3]-[6].

VI.SIMULATION RESULTS

6.1 Space Vector Pulse Width Modulation

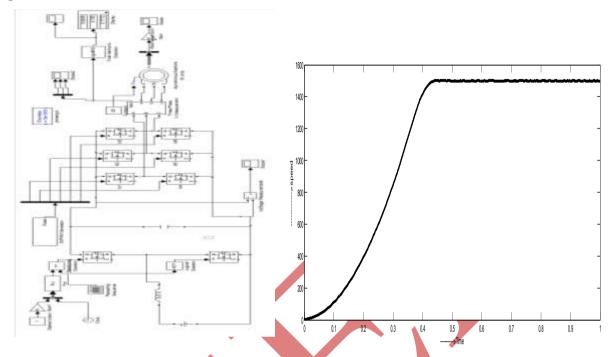


Fig 11. Simulation Circuit For SVPWM Inverter

Fig 11.1. Speed Of SVPWM Inverter Fed
Synchronous Machine

A buck boost converter in the front end is used to provide DC input at desire voltage levels. The space vector PWM is for providing gate signals to the thyristors. The harmonic content of the inverter output can be reduced using this technique. The output of the inverter is fed to load. The motor performance is superior in this case and it provides smooth speed control. Here, the speed waveform is with very less ripples and speed control is better when compared to the methods discussed before. The voltage and current waveforms are analysed in the further section.

6.2 Voltage & Current Analysis Of SVPWM

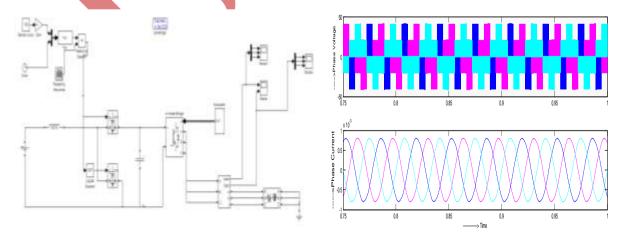


Fig 12. Simulation Circuit For SVPWM Inverter

Fig 12.1. Voltage And Current Of SVPWM Inverter

6.3 Closed Loop Control For Regulation Of Speed

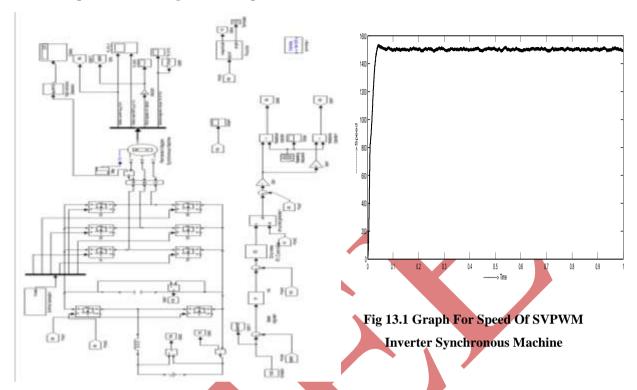


Fig.13. Simulation Circuit For Closed Loop Control For Speed Regulation

The speed control or regulation can be obtained using a closed loop feedback for an inverter fed machine. The speed from the output is taken and compared with a reference to give the error signal to a PI controller. The signals generated will be used to control the switching action of the chopper. This controls the output of the inverter which regulates the speed of the machine. Hence, with the execution of the above circuit, the speed can be well maintained. The above feedback control can be applied to any kind of multilevel inverter control

Table 1. Comparison Table

S.	PWM	THD	SETTLING
No		(%)	TIME
			(sec)
1.	Sinusoidal	1.09	0.12
	PWM		
2.	SVPWM	0.8	0.42
3.	Closed	0.5	0.84
	loop		
	control (PI)		
4.	Closed	0.29	0.04
	loop for		
	speed		
	regulation		

The speed regulation obtained by implementing SVPWM along with PI controller closed loop for the switching of Buck-Boost chopper. The purpose of Buck-Boost chopper at the front end of the inverter is to change the inverter input voltage as per the load variations or voltage variations, so as to maintain speed of the machine which is fed by this inverter to be maintained constant at a value set by the reference speed. By an implementing PI-closed loop control technique, this can improved the settling time (0.04 sec) than the normal svpwm method (0.42 sec) and also it has less total harmonics distortion 0.29% only.

Whenever the input voltage of the chopper is less than that voltage required to maintain the speed, then the chopper performs the Boost action to obtain the actual voltage at the inverter input to maintain the required speed.

Whenever the input voltage of the chopper is more than that voltage required to maintain the speed, then the chopper performs the Buck action to obtain the actual voltage at the inverter input to maintain the required speed.

3) Whenever the input voltage of the chopper is same as the voltage required to maintain the speed, then the chopper just isolates the actual DC input and the inverter input to maintain the required speed.

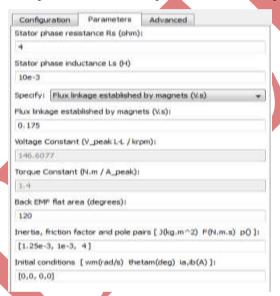


Fig.14. Synchronous Machine Parameters

XII. CONCLUSION

Comparison has been made to observe the THD in the inverter output with respect to different PWM techniques applied. The space vector PWM technique was found to give a better performance with less THD compared to other techniques. Instead of using a constant DC input to the inverter, a buck boost converter has been connected at the front end of the inverter. Therefore the same circuit can be employed for different AC loads connected to the inverter. The inverter output voltage can be varied according to the load requirements by varying the input to the inverter. This is done by varying the duty cycle of the chopper circuit in proportion to the load ratings. The PWM technique along with the closed loop control using the PI controller has lead to the reduction of the THD. Hence, such efficient PWM techniques are employed to the inverter which feed the AC machines so as to control the speed and torque. The ripples in the speed waveform are very less in this technique compared to open loop PWM techniques. Also the closed loop control using the speed feedback has been

implemented for the SVPWM inverter fed by chopper. The performance is better with less settling time and less harmonics in the output.

XIII. FUTURE SCOPE

The proposed SVPWAM modulation method has only been verified on the voltage source inverter. Thus the future work should be done with the buck-boost current source inverter—such as current-fed quasi-Z-source inverter topology. The discontinuous operation mode needs to be explored further to see if it can be utilized in order to bring some good features for the inverter, like higher boost ratio. For the circuit proposed, the chopper control circuitry can be provided with a closed loop control so as to maintain the inverter input constant irrespective of the load variations.

REFERENCES

- [1] Q. Lei and F. Z. Peng, "Space Vector Pulsewidth Amplitude Modulation for a Buck-Boost Voltage/Current Source Inverter," IEEE transactions on power electronics, vol 29, no. 1, Jan 2014.
- [2] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high power applications," IEEE Trans. Ind. Appl., vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.
- [3] W.McMurray, "Resonant snubbers with auxiliary switches," IEEE Trans. Ind. Appl., vol. 29, no. 2, pp. 355–362, Mar./Apr. 1993.
- [4] J. S. Kim and S. K. Sul, "New control scheme for ac-dc-ac converter without dc link electrolytic capacitor," in Proc. 24th Annu. IEEE PowerElectron. Spec. Conf., Jun. 1993, pp. 300–306.
- [5] K. Rigbers, S. Thomas, U. Boke, and R. W. De Doncker, "Behavior and loss modeling of a three-phase resonant pole inverter operating with 120°A double flattop modulation," in Proc. 41st IAS Annu. Meeting IEEE Ind.Appl. Conf., Oct. 8–12, 2006, vol. 4, pp. 1694–1701.
- [6] J. Shen, K Rigbers, C. P. Dick, and R. W. De Doncker, "A dynamic boost converter input stage for a double 120° flattop modulation based three phase inverter," in Proc. IEEE Ind. Appl. Soc. Annu. Meeting, Oct. 5–9, 2008, pp. 1–7.
- [7] H. Fujita, "A three-phase voltage-source solar power conditioner using a single-phase PWM control method," in Proc. IEEE Energy Convers.Congr.Expo., 2009, pp. 3748–3754.
- [8] H. Haga, K. Nishiya, S. Kondo, and K. Ohishi, "High power factor control of electrolytic capacitor less current-fed single-phase to three-phase power converter," in Proc. Int. Power Electron. Conf., Jun. 21–24, 2010, pp. 443–448.
- [9] X.Chen and M. Kazerani, "Space vectormodulation control of an ac-dc-ac converter with a front-end diode rectifier and reduced dc-link capacitor," IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1470–1478, Sep. 2006.
- [10] M. Hinkkanen and J. Luomi, "Induction motor drives equipped with diode rectifier and small dc-link capacitance," IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 312–320, Jan. 2008.