International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

INPUT CURRENT RIPPLE REDUCTION USING MODIFIED SEPIC CONVERTER AS PREREGULATOR

Aily Santhosh[1], Ch.Usha Sri[2]

[1]*EEE Branch, Vaagdevi College of Engineering, Bollikunta, (India)*

[2]*EEE Department, Vaagdevi College of Engineering, Bollikunta, (India)*

ABSTRACT

The simulation analysis of a modified version of the SEPIC dc–dc converter used as preregulator operating in discontinuous conduction mode (DCM) is given in this project. The presented converter presents a low input current ripple operating in DCM, and also the switch voltage is lower than the output voltage. The switch voltage reduction will increase the converter reliability and a low drain-to-source on-resistance (R_{DS-on}) MOSFET may be used depending on the converter specification. Moreover, a digital control technique is applied to the presented converter in order to reduce the third-harmonic input current distortion resultant of the operation in DCM.

Index Terms: *AC–DC power conversion, digital control, rectifiers.*

I. INTRODUCTION

The usual solution for the implementation of a high power factor (HPF) pre-regulator for a low-output power application is to use a boost converter operating in discontinuous conduction mode (DCM) [1], [2]. this can be a simple and cost-effective solution because the design of the rectifier in DCM allows the converter to operate as a voltage follower, wherever the input current naturally follows the input voltage profile while not the use of a current-control loop. The operation in DCM reduces the commutation losses since the switch turn-on occurs with zero-current switching (ZCS), and also the output diode doesn't present reverse recovery current. This solution is limited for low-power applications because of an increased converter conduction losses operating in DCM.

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

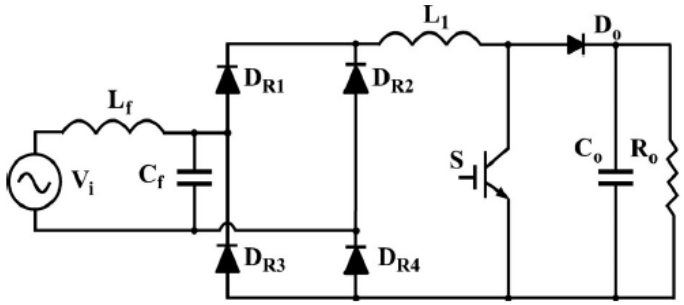

Fig. 1. Classical boost preregulator operating in DCM.

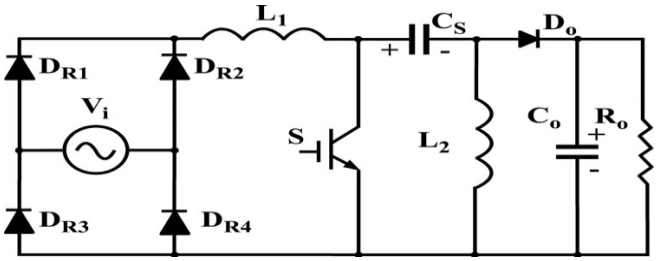

Fig. 2. Classical SEPIC preregulator operating in DCM.

Since the input inductor of the boost converter operates in DCM, a high-frequency filter composed by an inductor lf and capacitor C_f should be used in the pre regulator input in order to reduce the input current ripple, as given in Fig. 1. However, a problem given by the boost pre-regulator operating in DCM is the input current distortion, presenting a third-harmonic component.

The classical SEPIC converter, shown in Fig. 2, presents a step-up/step-down static gain and usually is employed as an HPF preregulator in applications wherever the output voltage should be less than the peak of the ac input voltage [3], [4]. The implementation of the preregulator using the classical SEPIC converter in DCM presents two further operation characteristics. Firstly, the converter operates as a voltage follower once designed in DCM with a low value for the inductor L_2 and employing a high value for the inductor L_1, however the input current presents a low current ripple just as a boost rectifier operating in CCM with current-control loop. Consequently, the l_f –C_f filter employed in the boost converter input operating in DCM isn't necessary using the SEPIC converter operating in DCM. Therefore, the number of components for both converters operating in DCM is equal. However, during a practical application, an electromagnetic interference (EMI) filter is important as in any rectifier topology.

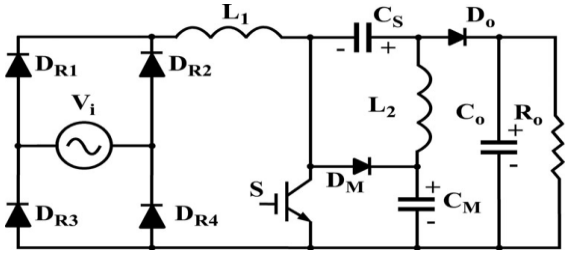

Fig. 3. Modified SEPIC preregulator operating in DCM.

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

The second important characteristic using the SEPIC converter in DCM is that the input current follows the input voltage wave form while not input current distortion. The third-harmonic distortion isn't given because the inductor L_2 is demagnetized with the output voltage.

The use of the boost and modified SEPIC rectifiers are only possible in applications with an output voltage higher than the peak of the input voltage, and these rectifiers are additional taken over than the SEPIC convertor with constant specification, since the SEPIC convertor presents a high switch voltage.

The modified SEPIC converter operates as a voltage follower and also the input current presents low current ripple like a classical SEPIC converter, designing the converter in DCM and employing a low value for the inductor L_2 and a high value for the inductor L_1. The main converter characteristics and analyses are given in the following, with the theoretical operation development of the presented converter.

II. THEORETICAL ANALYSIS

The circuit of the preregulator employing the modified SEPIC converter operating in DCM is given in Fig. 3. the main difference from the preregulator given the operation mode and also the control system that's composed by only a voltage control loop because of the DCM operation. Also, the non dissipative current snubber used isn't necessary because the reverse recovery current of the diodes and also the turn-on switching losses operating in CCM are reduced with the DCM operation.

The modified SEPIC dc–dc converter operating in DCM presents three operation stages. The theoretical analysis is initially developed considering the operation as a dc–dc converter at steady state and all circuit components are considered ideal. The voltages across all capacitors are considered constant during a switching period, as an ideal voltage source. The DCM operation occurs when there's the third operation stage, wherever the power switch is turned off and also the currents in all diodes of the circuit are null. Therefore, the DCM operation occurs when D_o and D_M diodes are blocked before the switch turn-on.

The operation stages in DCM are presented as follows:

1) First Stage [$t_0 - t_1$] (see Fig. 4): During the conduction of the power switch *S*, the input inductor stores energy with the input voltage applied across L_1 (V_{L1}). The voltage applied across L_2 (V_{L2}) is equal to the voltage of capacitor C_M minus the voltage of capacitor C_S . As presented in (1), this voltage difference is equal to the input voltage. Therefore, inductors L_1 and L_2 store energy in this operation stage and the same voltage is applied across these inductors. The currents through inductors L_1 and L_2 increase following (3) and (4), respectively, but since L_2 is lower than L_1 , the current variation in L_2 is higher than in L_1 , as presented in the theoretical waveforms shown in Fig. 7.

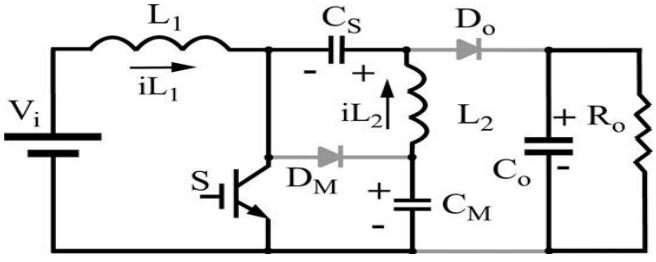

Fig. 4. First operation stage.

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

2) Second Stage [$t_1 - t_2$] (seeFig. 5): At the instant t_1 , switch S is turned off and the energy stored in the input inductor L_1 is transferred to the output through the C_S capacitor and output diode D_o . There is also energy transference to C_M capacitor through diode D_M and the maximum switch voltage is equal to the C_M capacitor voltage. The energy stored in inductor L_2 is also transferred to the output and capacitor C_S through diodes D_o and D_M . The voltage applied across L_1 is equal to C_M capacitor voltage minus the input voltage and this difference is equal to the C_S capacitor voltage as calculated by (1). The voltage across the inductor L_2 is equal to the negative capacitor C_S voltage. Thus, the voltage applied across the inductor L_1 and L_2 are equal to the negative capacitor C_S voltage during this operation stage and the inductor current variation is calculated by (6) and (7), respectively.

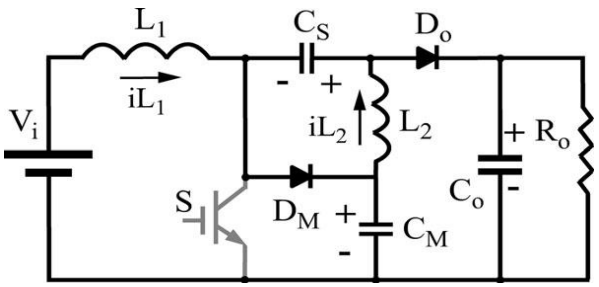

Fig.5.Second operation stage.

As presented in Fig. 7, the time interval (t_2–t_1) of the second operation stage is defined as *td* and is equal to the transference period of the energy stored in inductors L_1 and L_2 through diodes D_o and D_M . When L_2 current value becomes equal to L_1 current value with the same direction, the currents at Diodes D_o and D_M becomes null, finishing this operation stage. Therefore, t_d is the conduction time of diodes D_M and D_o , when the energy stored in the inductors L_1 and L_2 is transferred

$$V_{L_1} = V_{L_2} = -V_{C_S} \tag{1}$$

$$-\Delta i_{L_1} = \frac{-V_{C_S} \cdot D_{t_d}}{L_1 \cdot f} \tag{2}$$

$$-\Delta i_{L_2} = \frac{-V_{C_S} \cdot D_{t_d}}{L_2 \cdot f} \tag{3}$$

Where

$$D_{t_d} = \frac{t_d}{T} = t_d \cdot f. \tag{4}$$

3) Third Stage [$t_3 - t_4$] (see Fig. 6): When diodes D_o and D_M are blocked at the instant t_3 , the voltage applied across the inductors L_1 and L_2 are null, maintaining the inductors currents constant as presented in (9) and (10). The currents through the inductors L_1 and L_2 present the same value, operating as a freewheeling stage. This operation stage is finished when the power switch is turned on at the instant t_4 , returning to the first operation stage.

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

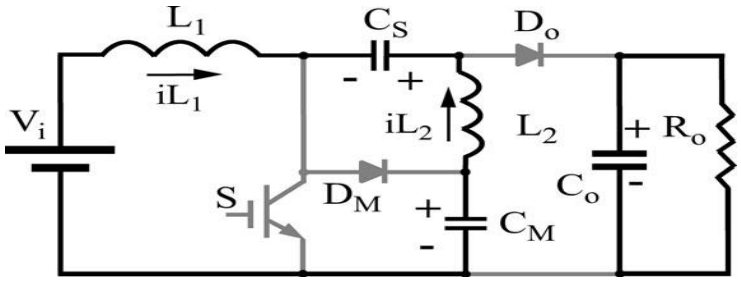

Fig. 6. Third operation stage.

$$V_{L_1} = V_{L_2} = 0 \tag{5}$$

$$\Delta i_{L_1} = \Delta i_{L_2} = 0. \tag{6}$$

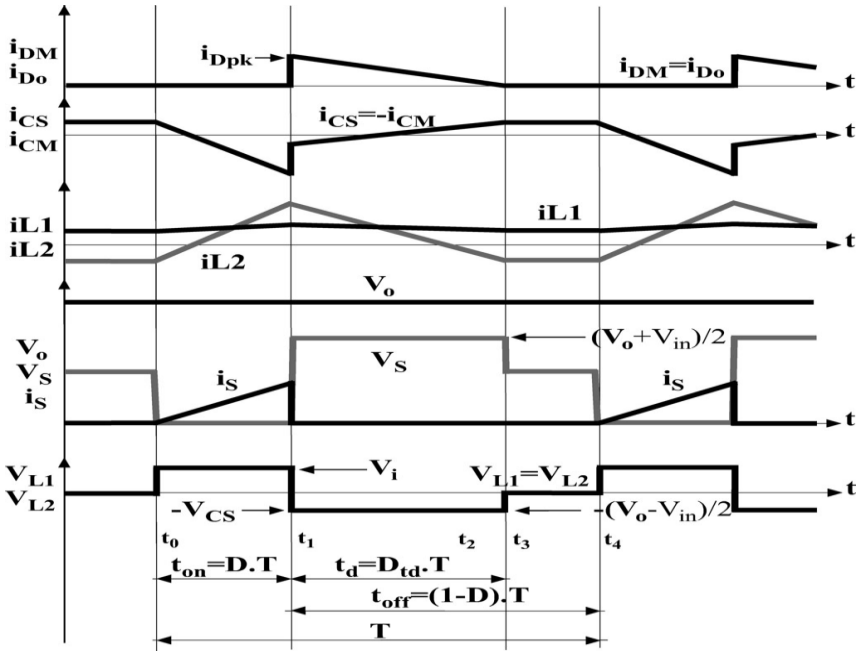

Fig. 7. Main theoretical waveforms.

The main theoretical waveforms are presented in Fig. 7. The switch turn-on occurs with ZCS such as a classical dc–dc converter operating in DCM and the diodes do not present reverse recovery current. The maximum switch voltage is equal to the capacitor C_M voltage, and this voltage is lower than the output voltage. The L_1 inductor average current is equal to the input current and the L_2 inductor average current is equal to the output current. The average current in the capacitors C_S and C_M are null at steady state; thus, the average current of diodes D_M and D_o are equal to the output current.

III. MATHEMATICAL ANALYSIS OPERATING AS A DC–DC CONVERTER

The main equations of the modified SEPIC converter, operating in DCM as a dc–dc converter with constant input voltage V_i are presented. Subsequently, a design procedure operating as preregulator with ac input voltage is presented based on the established equations.

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

3.1. Converter Static Gain and the Capacitors C_S and C_M Voltages

The output voltage is equal to the sum of the C_S and C_M capacitors voltages, as observed at the second operation stage presented in Fig. 5. The maximum switch voltage for the classical SEPIC converter is equal to the sum of the input and output voltages, while the switch voltage is equal to the output voltage for the boost converter. Considering the operation at steady state and the average voltage across the inductors as equal to zero, the theoretical waveforms presented in Fig. 7. The conduction period of the diodes t_d and the parameter D_{td} must be calculated for the static gain determination. As presented in Fig. 7, the currents at the diodes D_M and D_o are equal and the average value is equal to the output current I_o .

3.2. Limit for the DCM operation

The design procedure of the converter must ensure the operation only in DCM for any line voltage angle and in all operation conditions in order to maintain the HPF operation. The operation in CCM without current-control loop results in input current distortion increasing the total harmonic distortion (THD).

The conduction period of the power switch is represented by the interval ($t_1 - t_0$) in Fig. 7 and also by the converter duty cycle ($D{\cdot}T$). The conduction period of the output diode is defined by the interval ($t_2 - t_1$) and by the parameter (D_{td} T). The limit for the DCM operation occurs when the sum of the switch conduction period and the diode conduction period is equal to the switching period (T).

Table 1

Design Specifications

Parameter	Preregulator with Modified SEPIC Converter
Nominal input voltage (V_{irms})	$V_{irms} = 127$ V
Peak value of input voltage (V_{pk})	$V_{pk} = 180$ V
Output voltage (V_o)	$V_o = 400$ V
Output power (P_o)	$P_o = 100$W
Switching frequency (f)	30 kHz
Line frequency (f_L)	$f_L = 60$ Hz
Maximum input current ripple	$\Delta i_L = 26\%$ of the input peak current

IV. THIRD-HARMONIC REDUCTION TECHNIQUE

The classical boost rectifier operating in DCM and the modified SEPIC rectifier present a third-harmonic distortion in the input current. This current distortion is a function of the voltage difference between the input and output voltage. Normally, the output voltage is increased in order to reduce the third-harmonic distortion and to maintain HPF, but the semiconductors losses are increased.

The converter duty cycle must be changed in a half cycle of the ac input voltage in order to maintain constant, since the parameter D_{td} (ωt) changes with the input voltage. The parameter K_c should be calculated at each half cycle of the ac input voltage because this parameter is a function of the peak of the input voltage V_{pk} and also

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

changes with the output current. The variation of the main rectifier parameters with the input voltage as the duty cycle, conduction period of the output diode, input current, and the average value of the output diode current are presented for the operation with and without the third-harmonic reduction technique.

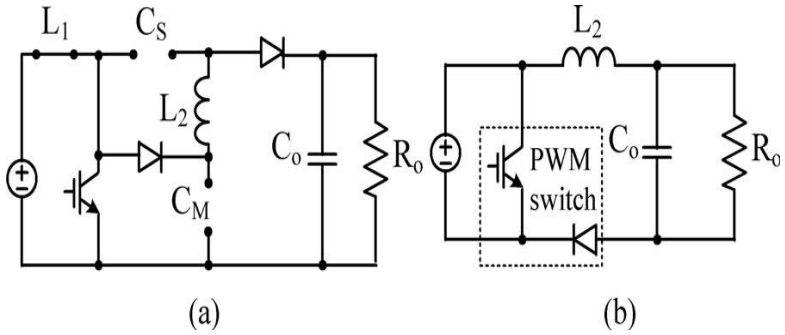

Fig.8. Simplified circuit model of modified SEPIC dc–dc: (a) with neglected components and (b) equivalent circuit.

V. OUTPUT VOLTAGE CONTROL SYSTEM

5.1.Control-to-Output Transfer Function [v_o (s)/d(s)]:

A dynamic model of switching converter is required for feedback control loop. However, the power converters are described by a set of the nonlinear differential equations. Usually, it is easier to analyze a small signals model that is linearized related to the quiescent operation point in order to obtain a linear model, as presented.

The small signal equivalent circuit of buck, boost, and buck– boost converters presents a capacitor and an inductor, operating in DCM. The transfer functions have two poles. One pole is due to the output capacitor, at low frequency, and other pole, in much higher frequency due to the inductor. For this reason, an approximate way to determine the low-frequency small-signal transfer function of the basics converters is to let the inductance tend to zero. Also, the capacitor C_M and C_S are very small in the modified SEPIC converter, where $C_o >> C_M$ and $C_o >> C_S$. Therefore, they can be neglected to obtain control-to-output transfer function for low frequency. In this case, the high-frequency capacitors dynamics can be ignored. The modified SEPIC without C_M, C_S , and L_1 is shown in Fig. 8(a) and the equivalent circuit is shown in Fig. 8(b). The remaining model is solved for the low-frequency converter dynamics.

Table 2

Preregulator Components

Parameter	Preregulator with modified SEPIC converter
Inductor L_1	$L_1 = 6.8$ mH, ESR = 692 mΩ
Inductor L_2	$L_2 = 540\ \mu$H, ESR = 98 mΩ
Capacitor C_S	$C_S = 220$ nF, ESR = 10 mΩ
Capacitor C_M	$C_M = 220$ nF, ESR = 10 mΩ
Output capacitor C_o	$C_o = 120\ \mu$F, ESR = 390 mΩ
Diodes $D_M - D_o$	$D_M = D_o =$ UF5408 $V_f = 1.7$V
Power switch S	$S =$ FQA28N50 $V_{DSS} = 500$ V $R_{DSon} = 0.16\Omega$ (25 °C)

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

VI. SIMULATION RESULTS

The presented preregulator simulation model is shown in fig. 12 using the specifications presented in Table1, and the components used are shown in Table 2.

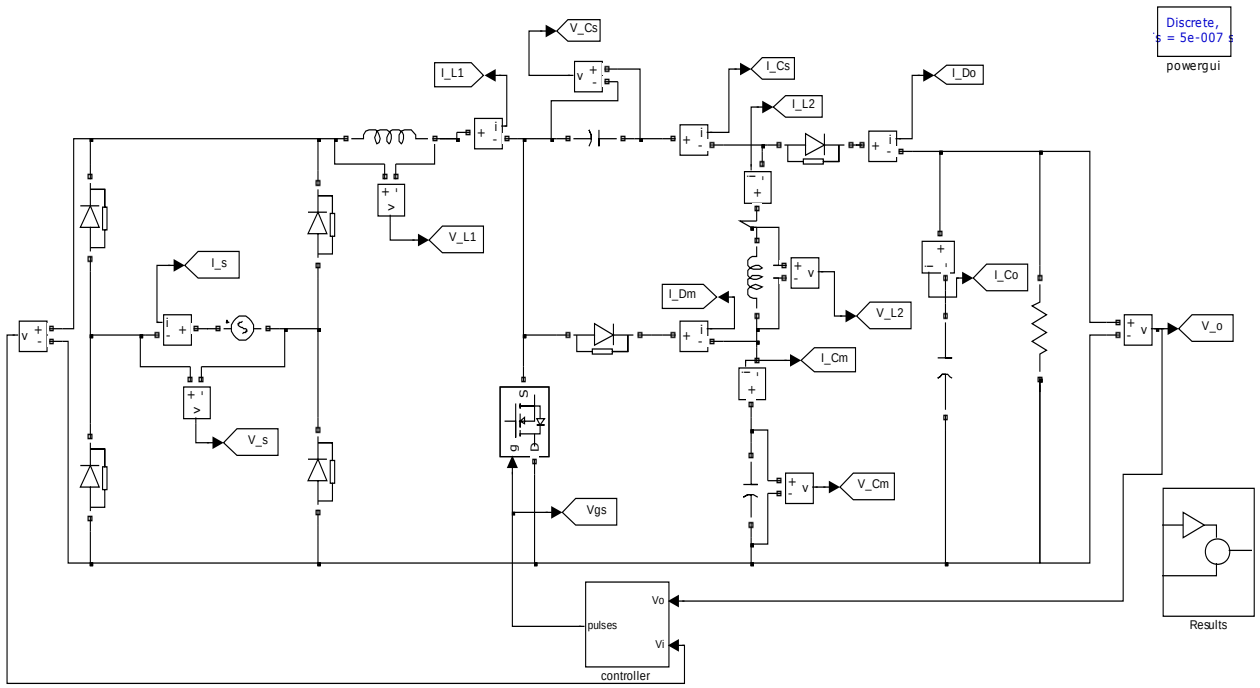

Fig.9 Simulation model

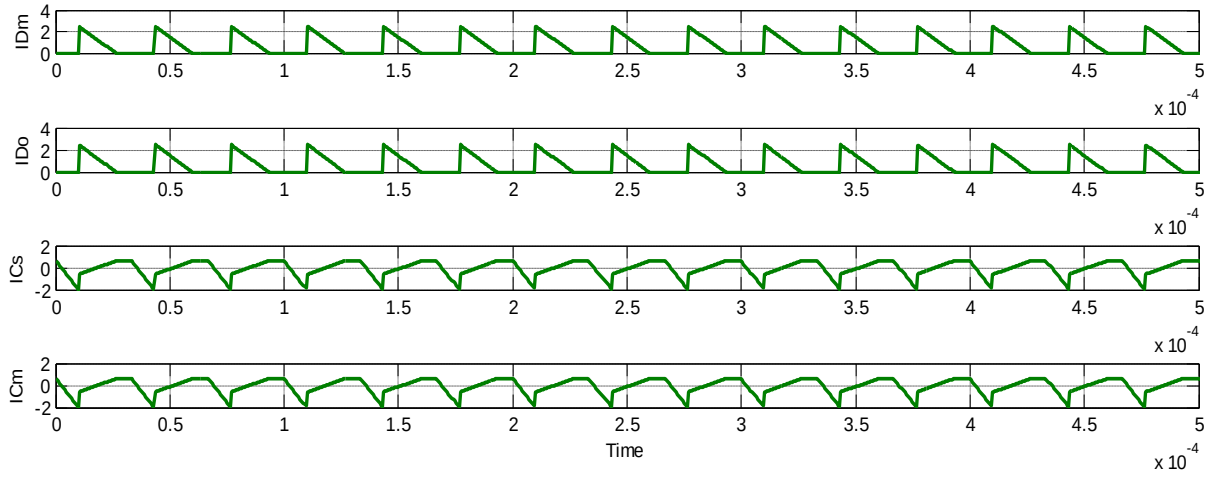

Fig10. Simulation results for I_{Dm}, I_{Do}, I_{Cs} and I_{Cm}

During the conduction of the power switch S, the input inductor stores energy with the input voltage applied across L_1 (V_{L1}). The voltage applied across L_2 (V_{L2}) is equal to the voltage of capacitor C_M minus the voltage of capacitor C_S. As presente, this voltage difference is equal to the input voltage. Therefore, inductors L_1 and L_2 store energy in this operation stage and the same voltage is applied across these inductors. The currents through inductors L_1 and L_2 increase following (3) and (4), respectively, but since L_2 is lower than L_1, the current variation in L_2 is higher than in L_1, as presented in the theoretical waveforms shown in Fig.10

International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

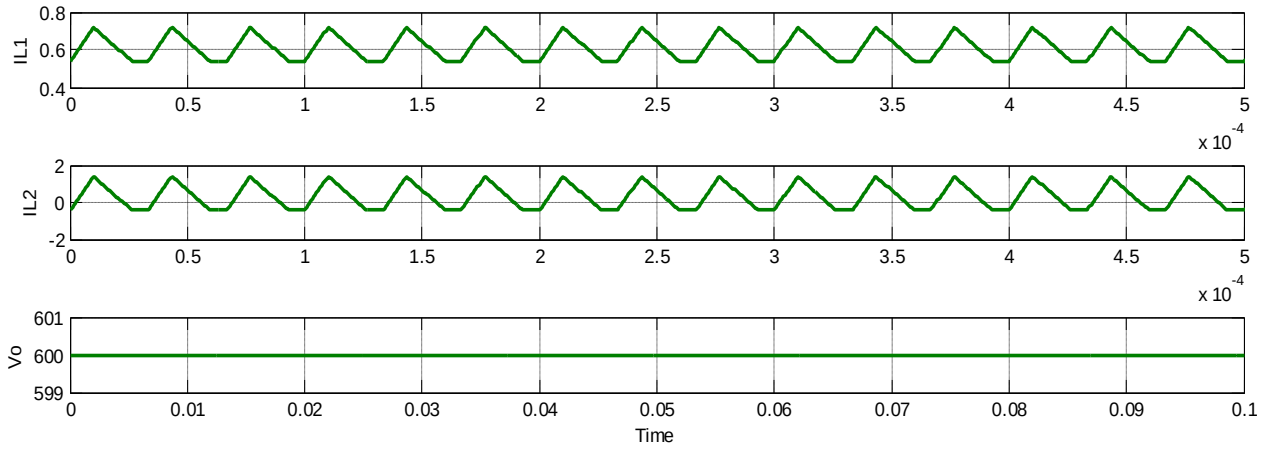

Fig.11 Simulation results for I_{L1}, I_{L2} and V_o

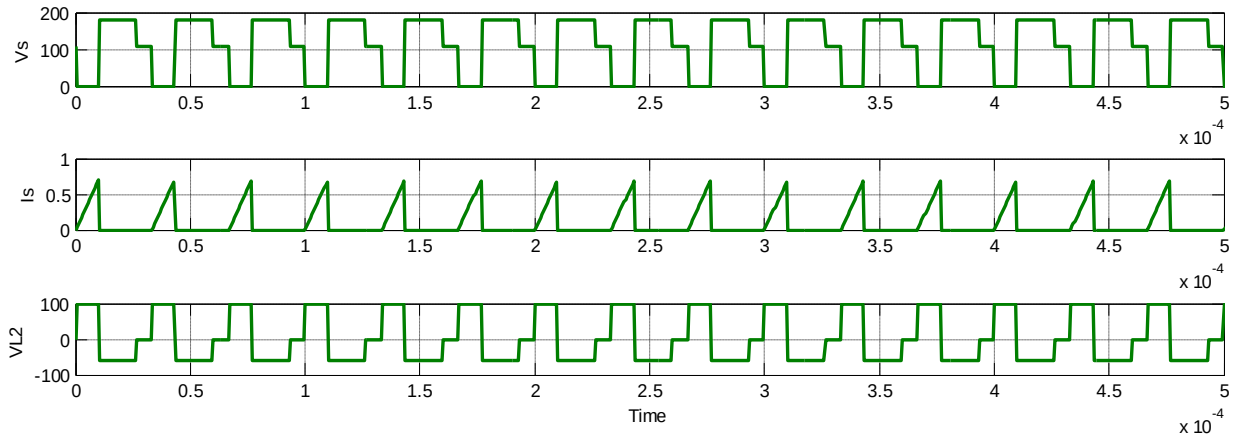

Fig.12 Simulation results for V_s, I_s and $_{VL2}$

As presented in Fig. 11, the time interval (t_2–t_1) of the second operation stage is defined astd and is equal to the transference period of the energy stored in inductors L_1 and L_2 through diodes D_o and D_M. When L_2 current value becomes equal to L_1 current value with the same direction, the currents at diodes D_o and D_M becomes null, finishing this operation stage. Considering the operation at steady state and the average voltage across the inductors as equal to zero, the theoretical waveforms presented in Fig.12 shows that the positive area of the inductor voltage must be equal to the negative area as presented in (5) for the inductor L_1.

VII. CONCLUSION

The theoretical and Simulation analysis of the modified SEPIC converter used as preregulator operating in DCM is given during this project. The presented converter presents low input current ripple operating in DCM and also the switch and diodes voltages are lower than the output voltage. The switch voltage reduction will increase the converter reliability and a lower $R_{DS\text{-}on}$ MOSFET may be used depending on the converter specification.

The simulation results given operating with the third harmonic reduction technique shows that the total input current harmonic distortion is reduced from 13 to 5.3% operating with an input voltage equal 127 V_{rms} and is

reduced from 35.9% to 8.84% operating with an input voltage equal to 220 V_{rms} , considering a total input voltage harmonic distortion equal to 3.1%. the power factor is higher than 0.988 with the third harmonic reduction in all input voltage range. The efficiency operating with input voltage equal to 127 V_{rms} and output power equal to 108W is equal to 95.6%. The simulation results show that there's also an increment in the converter efficiency operating with the third-harmonic reduction modulation that mainly occurs at light load operation in 127 and 220 V_{rms} .

REFERENCES

[1] O. Garc´ıa, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 749–755, May 2003.

[2] M.M. Jovanovic andY. Jang, "State-of-the-art, single-phase, active powerfactor- correction techniques for high-power applications—An overview," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 701–708, Jun. 2005.

[3] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and CUK power factor preregulators: Analysis and design," IEEE Trans. Ind. Electron., vol. 44, no. 5, pp. 630–637, Oct. 1997.

[4] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[5] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[6] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56, no. 4,pp. 1147–1157, Apr. 2009.

[7] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless pfc rectifier with simple zero-current detection and full-range zvs operating at the boundary of DCM/CCM," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 427–435, Feb. 2011.

[8] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," IET Power Electron., vol. 5, no. 3, pp. 358–365, Mar. 2012.

[9] Y. Cho and J.-S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless pfc converters," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 165–175, Jan. 2013.

[10] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Bridgeless resonant pseudo boost PFC rectifier," IEEE Trans. Power Electron., vol. 29, no. 11, pp. 5949–5960, Nov. 2014.