International Journal of Electrical and Electronics Engineers
Vol. No. 8, Issue No. 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321-2045

PERFORMANCE ANALYSIS OF CLA CIRCUITS USING SAL AND REVERSIBLE LOGIC GATES FOR ULTRA LOW POWER APPLICATIONS

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ABSTRACT

Low power design has become one of the primary focuses in both analogue and digital VLSI circuits. Many power consumption techniques have come in existence and with that the low power design is also achieved by scaling supply voltage, considering sub-threshold region in this region thereby obtaining a minimum energy consumption which also suits for low operating frequencies. In this paper proposed for comparing the sub threshold logics and reversible logics power dissipations. The reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The basic gates such as AND, OR, and EXOR are not reversible. This paper presents various designs of reversible logic gates used for reversible operation & the applications as carry look ahead adder and select adder Block. This paper also includes simulation result of reversible TSG, pers & Toffoli gate. These gates are then used to design four bit Carry look ahead adder and select Adder blocks. Methodology used for designing reversible gate is Tanner Tool Version-13.0technologyfile0.18micron

Keywords: *SAL, Reversible logic, Quantum Cost, low power carry look ahead adder.*

I. INTRODUCTION

Recently, adiabatic logic (or energy recovery logic) [5]–[8] style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime. Since the performance requirements are

many of these energy efficient sub-threshold applications [1], [2], we believe that the adiabatic style can be used efficaciously in a sub-threshold regime to make the circuit more energy efficient.

Sub-threshold logic aims at low is not allowed in reversible logic, this gate is useful for duplication of the required outputs. power consumption, which is usually constrained to a few tens of Watts. In case of temperature variations, sub-threshold current will vary as it depends exponentially on temperature. Therefore, output node swing can be affected due to the temperature variation SAL saves considerable energy compared with the static conventional logic counterpart over a wide range of frequency. In particular, the impact of temperature variation on leakage dissipation, output swing.

The SAL Logic reduce the few amount power dissipation . here proposed for reversible logic using carry select adder for reducing power dissipation and delay. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1.

Any unitary operation is reversible hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logical components [3]. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors.

II. SUBTHROSHOLD LOGIC DESIGN

The subthreshold current always flow from source to drain even if Vgs is lesser than Vth of the device. This happened due to carrier diffusion between source and drain regions of the CMOS transistor in weak inversion. The subthreshold current become significant current Isub, which occurs when Vgs is below Vth, is the main part of the leakage current. It has also been investigated that off state current occurs due to gate leakage near the drain region of the device and experimental manipulation states that it increases with the increments in number of transistors of the chip. It is estimated that the silicon oxide can scale down to the 1.4 to 1.5 nm regime for high performance application. The off-state leakage will remain within the target specifications (nA/ m). However for low power application gate leakage dominates the gate oxide issues with respect to scaling silicon oxides, for that oxide thickness may be limited to 1.8 to 2.0 nm regime with the reduction of the off-state power consumption and maintain an acceptable level of charge retention. Reliability will probably limit silicon oxide scaling for high performance applications whereas gate leakage will limit gate oxide scaling for low power and memory applications

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[12]. Direct tunneling phenomena of the discrete charges randomly crossing a potential barrier in the gate oxide thickness produces a non-negligible gate current. This leakage current is the main source of the static power consumption for digital circuits [13]. W.Kirklen et.al. describes about the significant consequences of the off-state leakage which occurs due to short channel effects.

II. MOTIVATION OF REVERSIBLE LOGIC GATES

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications.

To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored

2.1 Reversible logic

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible.However fan out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

The number of Reversible gates (N): The number of reversible gates used in circuit. The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

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2.2 Reversible Logic Gates

2.2.1 Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out.

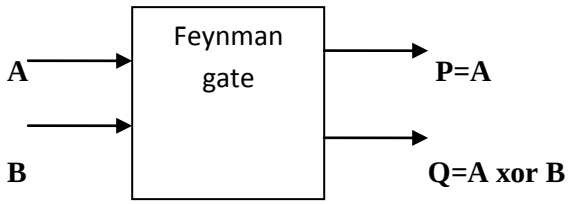

Fig:1 Feynman gate

Truth table:1

A	B	P	G
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2.2.2 Peres Gate

Fig shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AB and R=AB C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

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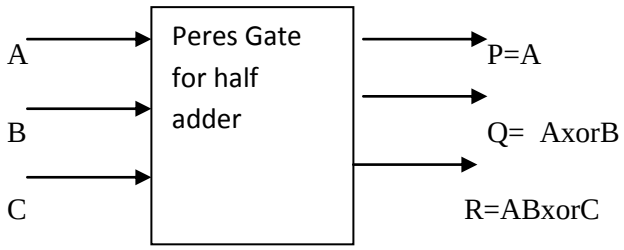

Fig:2 Peres gate

Truth table:2

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

A full- adder using two Peres gates is as shown in fig 3. The quantum realization of this shows that its quantum cost is 8 two Peres gates are used.

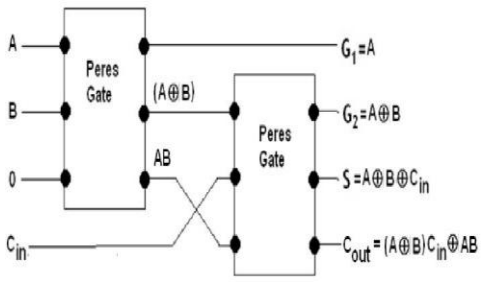

Fig:3 Full adder using peres gate

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2.2.3 Toffoli gates

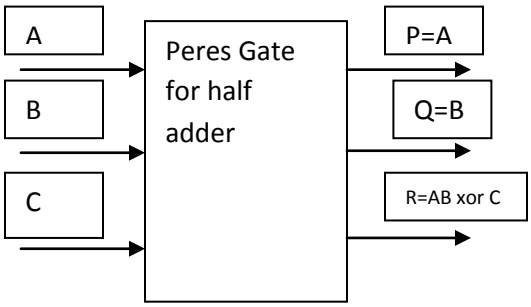

Fig: 4 Toffoli gates

The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB ⊕ C.

Truth table :3

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

III. PROPOSED 4 BIT CARRY LOOK AHEAD ADDER

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator andCarry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -

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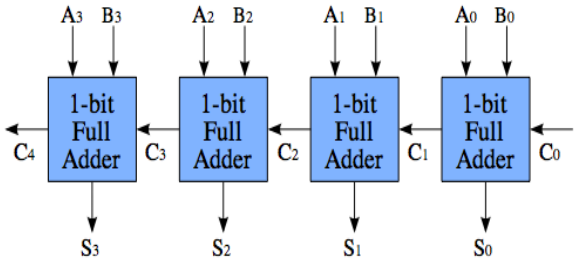

Fig:5 Carry look-ahead adder circuits

IV. RESULTS

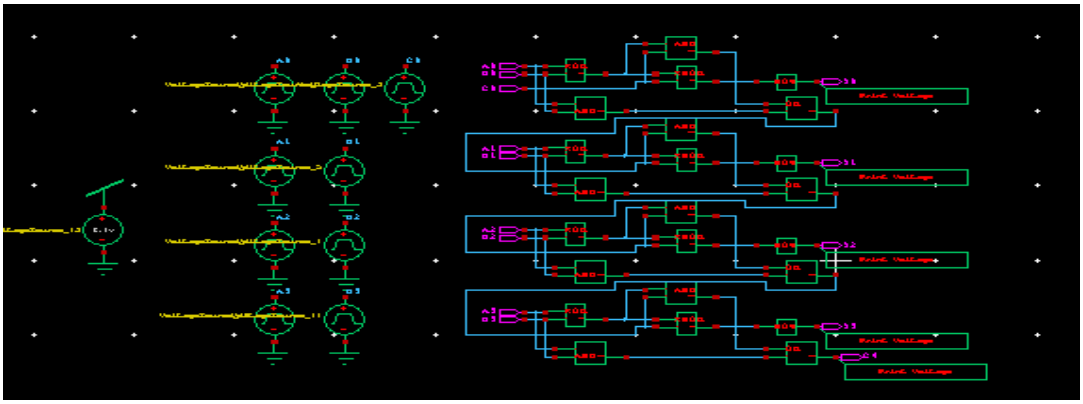

Fig :6 SAL based CLA Design

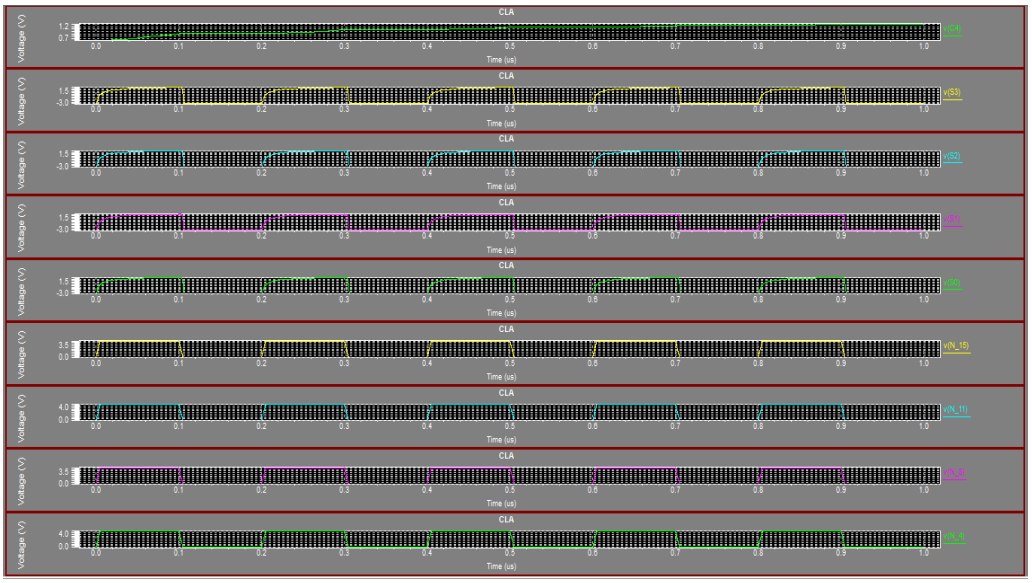

Fig: 7 Waveform For SAL CLA Logic

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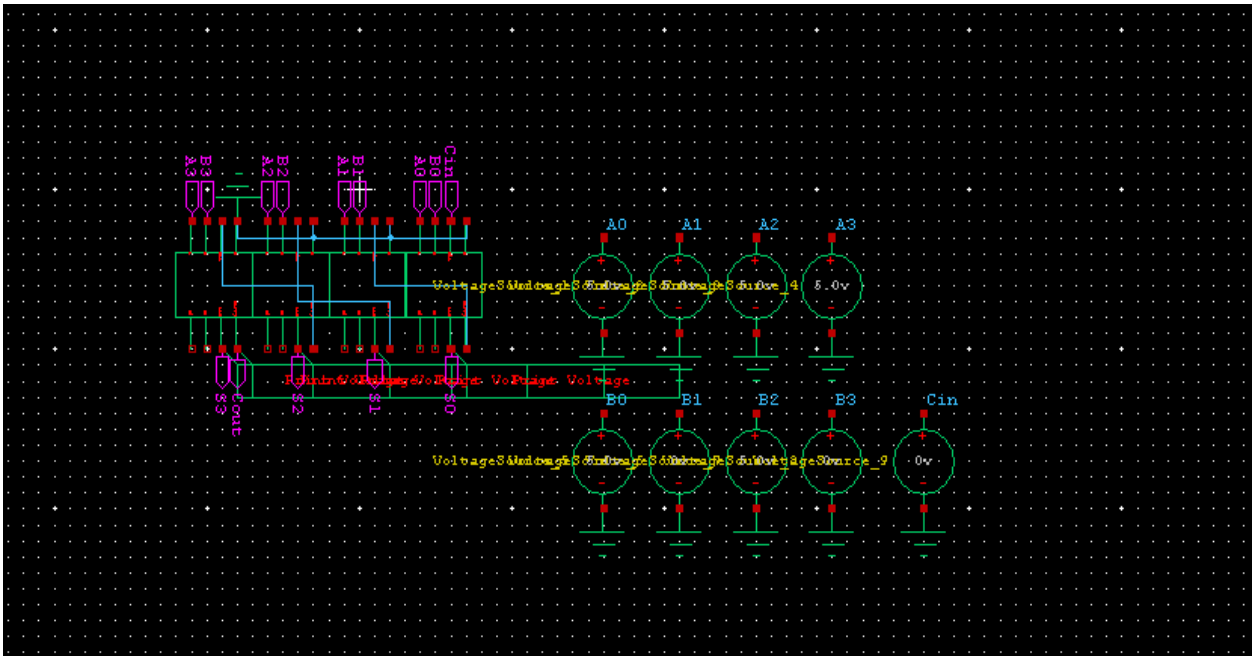

Fig: 8 Reversible logic Using CLA Design

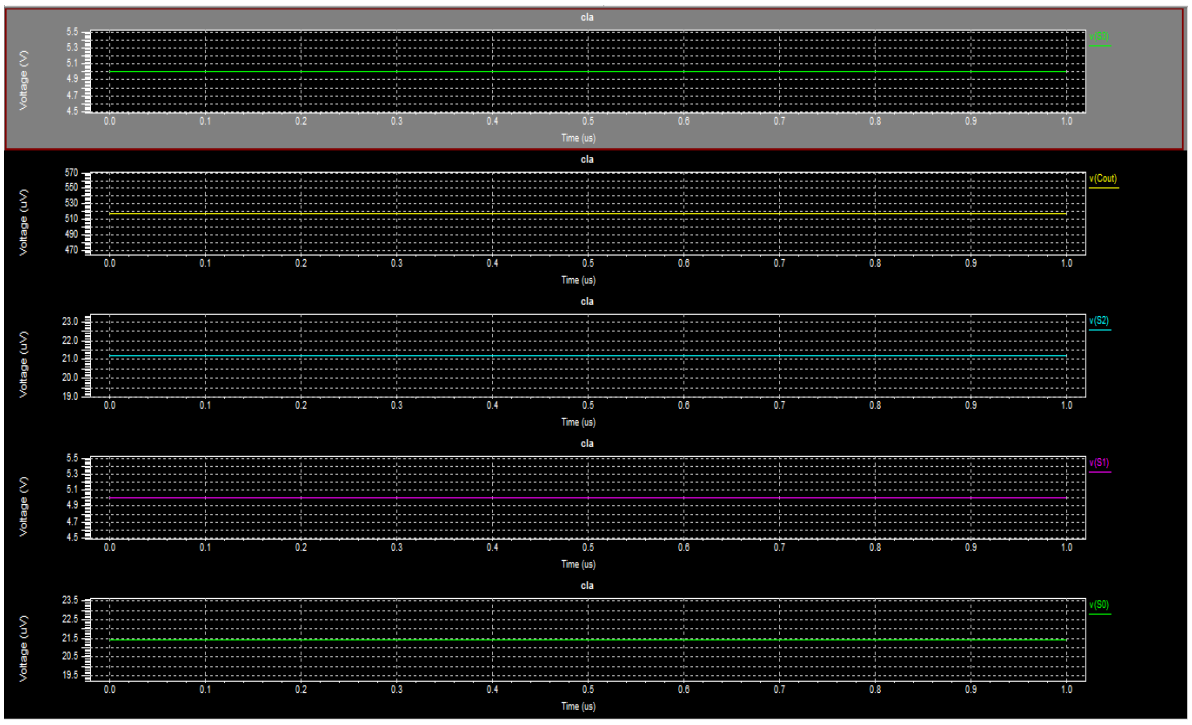

Fig:9 Waveform for Reversible Logic CLA

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V. POWER ANALYSIS

Types	Power consumption
SAL CLA Design	3.200101e+002 watts
Reversible logic base CLA design	5.670659e-007 watts

VI. APPLICATIONS

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1. Low power CMOS.

2. Quantum computer.

3. Nanotechnology

4. Optical computing

5. Design of low power arithmetic and data path for digital signal processing (DSP).

6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

VII. CONCLUSION

The focus of this paper is on transistor implementation of reversible 4*4 carry look-ahead adder circuit. The proposed design offers less area and less power consumption compare to SAL logics. In future we are planning designing the CSA adder using reversible logic gates.

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