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IMPLEMENTATION OF MULTIRATE SAMPLING ON FPGA WITH LOW COMPLEXITY FIR FILTERS

Prof. R. V. Babar[1], Pooja Khot[2], Pallavi More[3], Neha Khanzode[4]

[1, 2, 3, 4] *Department of E&TC Engineering, Sinhgad Institute of Technology, Lonavala, (India)*

ABSTRACT

Multi-rate Signal Processing includes the study of multiple sample rates within a system in order to achieve computational efficiencies which are impossible to obtain with a system that operates on only fixed sample rate. Multi-rate Signal processing uses the study of sample rate conversion which is the part of Digital Signal Processing. This method is used for systems with dissimilar input and output rates, however may also be used to implement systems with equal input and output sample rates. Field Programmable Gate Array (FPGA) offers good solution for addressing the needs of high performance DSP systems. The focus of this paper is on the proposed architecture of Multirate signal processing circuits which are Interpolator and Decimator with low complexity.

Keywords– Decimator, FPGA, FIR, Interpolator, Polyphase Decomposition.

I. INTRODUCTION

Multirate Digital Signal Processing finds wide range of application in fields such as, telecommunications, image enhancement and processing, digital TV broadcasting, voice synthesis and recognition, speech signals, and many other fields. In multirate methods, decimator and interpolator filters are the most important building blocks [1]. Digital filters have advantages over analog filters- flexibility, versatility, high precision, reliability. The speed of processing and an area are the very important factors in the VLSI application and hence a scalable implementation system to implement the multirate FIR filters flexibly and efficiently is presented in this paper. The complexity of the circuit is increased if used ordinary FIR filters. To reduce the overall complexity of the Interpolator and decimator circuit we use low complexity FIR filter design by using PSM (Programmable Shift Method) architecture.

In this paper, we present an efficient approach for the low-power design of a linear time-invariant (LTI) FIR/IIR method which is based on the multirate method. The direct implementation of the system transfer function H (z) (Fig. l) is shown. It has the constraint that it cannot compensate the speed penalty under lower supply voltage. On the other hand, the processing elements are able to operate at a low supply voltage in order to reduce the power dissipation and the data throughput rate is not corrupted by the lowered voltage as the multirate system will lower the speed of processing elements at half of the original clock rate so as to maintain the same throughput. Thus the multirate implementation provides a direct and effective method to compensate the speed drawback in low power designs.

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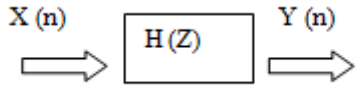

Figure.1 LTI FIR/IIR system

Multirate filters are needed for changing the sampling rate of a data path in a system. Multirate filters contain interpolation as well as decimation filter. Interpolator increases the sample rate by introducing zero valued samples in between the original samples. Decimator removes the samples in order to decrease the sample rate. The FIR Compiler creates interpolation and decimation filters by using polyphase decomposition [2]. Polyphase filters simplify the overall system design. It also decrease the number of computations per cycle which is required by the hardware.

II. DESIGN ASPECTS

2.1 Interpolation filters

An interpolation filter enhances the output sampling rate by a factor of I through a process known as zero padding. It consists of insertion of I-1 zeros between input samples. Polyphase decomposition decreases the number of processes per clock cycle by ignoring the zeros that are inserted in between the original input samples. Polyphase interpolation filters deliver both speed and area optimization. This is because each polyphase filter runs at the input data rate for maximum throughput.

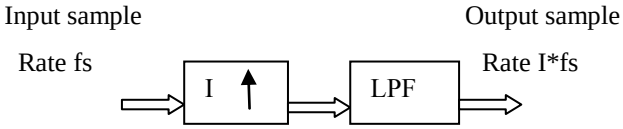

Figure. 2(a) Interpolation Filter Block Diagram

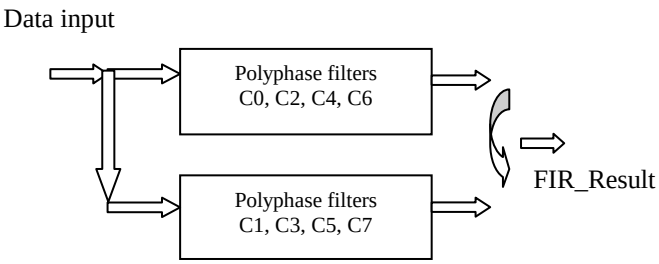

Figure2. (b) Polyphase Interpolation Block Diagram

2.2 Decimation filters

A decimation filter reduces the output sampling rate by a factor of D by retaining only every D^{th} input sample. Polyphase decomposition decreases the number of operations per cycle. It ignores the input data samples which are removed during down sampling. As each polyphase filter operates at the output data rate, polyphase decimation filters deliver speed optimization.

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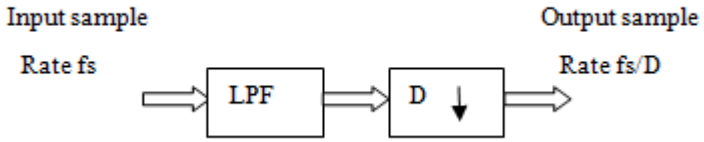

Figure3. (a) Decimation Filter Block Diagram

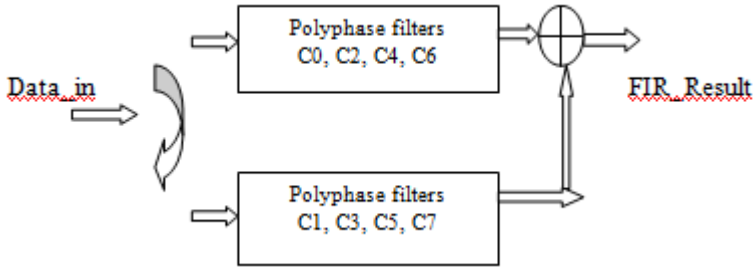

Figure3. (b) Polyphase Decomposition for Decimation filters

2.3 Filter design

FIR filters have wide applications in mobile communication systems because of their complete stability and linear phase properties. The difficulty of FIR filters is controlled by the complexity of coefficient multipliers. In this paper, we use architecture that combines reconfigurability and low complexity to realize FIR filters [6]. The FIR filter design which used is Programmable Shifts Method (PSM). The design and analysis of the architecture is presented

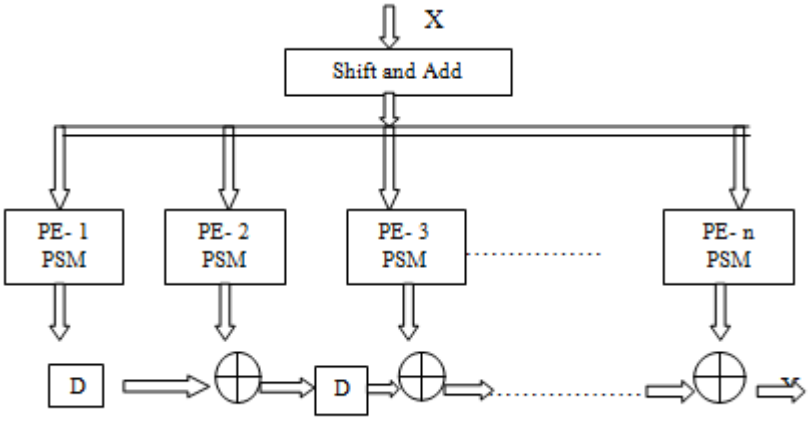

Figure.4 Transposed Direct Form of FIR filter

In this unit, the design of the used FIR filter is presented. The architecture is based on the transposed direct form of FIR filter structure as shown in Figure.4. The dotted portion in the Figure.4 denotes the MB and PE-i represents the processing element equivalent to the i^{th} coefficient. PE performs the coefficient multiplication with the help of a shift and add unit. In the construction of PE for PSM, the PE contains Programmable Shifters (PS). The FIR filter architecture can be understood in a serial way in which the same PE is used to generate all partial products through convolving the coefficients with the input signal ($h * x[n]$). It can also be realized in a parallel way, where parallel PE architectures are used. The basic architecture of the PE for FIR Filter is shown in Fig.5.

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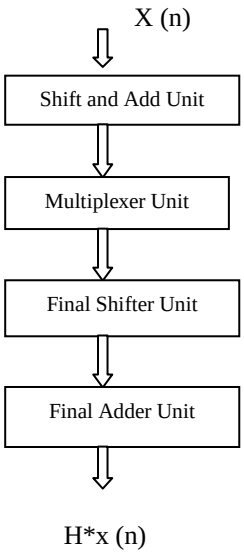

Figure5. Block Diagram for Architecture of PE for FIR filter

III. SIMULATION RESULTS

3.1 Interpolator

It is possible to achieve multi rate sampling by using Interpolator at input side. The drawback of this technique is that complexity is increased. In order to reduce the complexity we use low complexity FIR filters. This is reduced by designing FIR filter by using shift and add module along with programmable shifting method. Simulation Results of Interpolator Module is depicted in the following Fig.9.

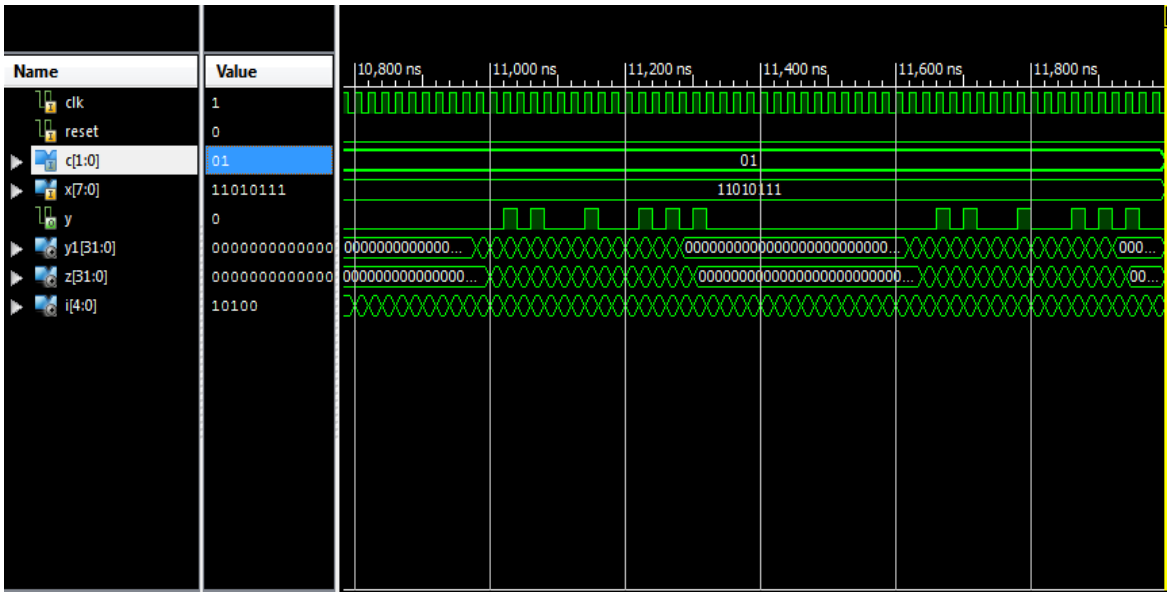

Figure6. Simulation result of Interpolator module

From the simulation results it is observed that as per the definition of interpolation zero padding is done among the samples. Here X (n) is 8 bit input and y is the output.

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IV. FPGA IMPLEMENTATION

The proposed design is targeted on to Xilinx SPARTAN-3 FPGA device with a speed grade of -4. It is observed that above 40% area for the targeted FPGA is covered for the implementation of this system. The CLB'S are connected in cascade manner in order to obtain the functionality of the designed system [4].

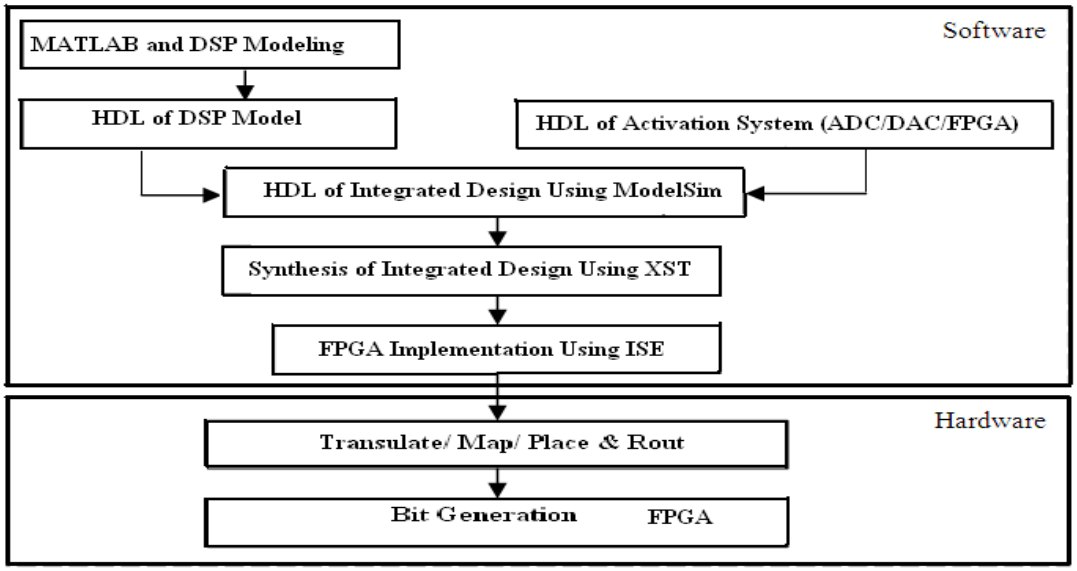

Figure7. FPGA Design flow

V. RESULTS AND DISCUSSION

In this paper, we have presented FIR filters which are applicable for multirate sampling by using interpolator and decimator [5]. For reducing the complexity we have used the low complexity FIR filter design with the help of programmable shifting method (PSM).

Advantages

The advantages of this work are:

- Reduced complexity
- Reduces area
- Reduced power dissipation
- High throughput rate
- High processing speed
- Fast computation

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