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DESIGN OF A LOW-VOLTAGE AND LOW DROPOUT REGULATOR WITH ASSISTANT PUSH-PULL OUTPUT STAGE CIRCUIT

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ABSTRACT

The Low-Dropout regulator is driven by increasing number of low voltage applications require the use of LDO widely used in various integrated circuits these days such as cellular phones, pager, laptops and in many electronic applications. In this paper introduce design of a LDO with Assistant push-pull output stage circuit to enable ultra-power dissipation and reduce Dropout voltage is presented. To design LDO with APPOS circuit and avoid external on chip capacitor while achieving fast response and accurate regulation. The experimental result shows the LDO regulates output voltage at 1.3V from 1.5V supply voltage. The proposed LDO provides a clean supply deliver to the element, and also it attenuates the high frequency glitches, and significantly the performance of the circuit increase. Here we are designed undershoot and overshoot circuits with detection of over deliver signal and under deliver signal. In order to drive these types of circuits internally consists of same driving capability. The proposed LDO with assistant push-pull output stage circuit has been implemented by modifying the existing LDO techniques.Post layout simulations and comparisons are made for all these architectures where the proposed circuit has obtained much better dropout voltage when compare to the all existing schemes and the power consumption is slightly reduced. The circuit presents presented in this work are using the back-end tool H-Spice and are designed in 180-nm technology.

Keywords: Operational Amplifier, Low Dropout Regulator (LDO), Low Voltage , CMOS Analog Integrated Circuits, High Power Supply Rejection(PSR).

I. INTRODUCTION

Generally power management systems connect with so much integrated regulators in often used modern battery portable devices. The power management unit often using primary switching regulators and several post regulators are used. The primary switching regulator converts the high dc voltage level of the battery into a low dc voltage level with high conversion ratio. The Low dropout regulators are use in DC-DC converters, switching

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regulators. Switching regulators are mixed mode circuits that feedback an analog error signal and digitally gate provided of current to the output. Switching regulators can provide a wide range of output voltages that can be reduce or increase then the input voltage depending on the circuit configuration. The post regulators also generate several independent power source for multiple voltage controlled. The switching regulator prevent generates voltage ripples over the range of the switching frequency.

The switching frequency of the regulator often within a low frequency band of a few 10-100Khz to reduce switching power loss. The post regulators should, therefore be able to provide a good power supply rejection (PSR) ability to suppress these unwanted low-frequency noises. To further maintain high power efficiency, minimize impact on target load circuits, and reduce cost, the post regulators must operate at low voltage and low power consumption is achieve a fast response with a small output variation. The low dropout (LDO) regulator has a simple architecture and a fast responding loop.

Regulators are classified into two types there are linear regulator and nonlinear regulators, among this two the linear regulators are mostly used. Because this provides filter out the noise and provides a clean supply voltage to drive noise sensitive circuits such as transimpedance amplifier and low noise amplifier.

II. EXISTING LOW DROPOUT REGULATOR WITH DIFFERENT TECHNIQUES

2.1. Conventional LDO Based on the flipped Voltage follower Topology

Flipped voltage follower also called as source follower it can be depend single control based transistor. LDO based FVF is provide ultra-fast load conditions, and also provided stable voltage regulation. The conventional flopped voltage follower based on LDO which is shown in fig.1. Here using two inputs there are supply voltage and another one is reference voltage of the differential amplifier.

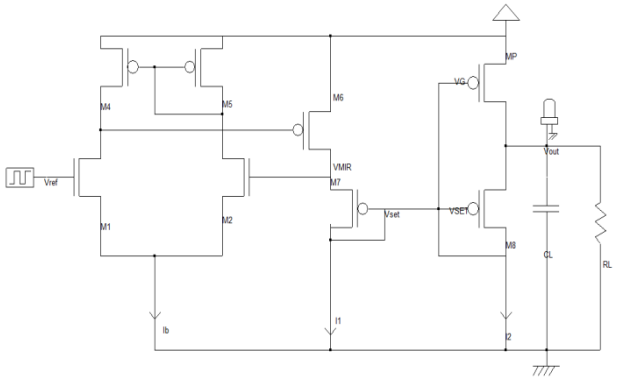

Fig.1 Schematic diagram of Conventional LDO based on Flipped voltage follower

LDO mainly consist of pass element, it pass device using PMOS transistor, because of which can be provides a power supply rejection is better with PMOS transistor. Differential operational amplifier using four stages there are input stage, differential stage, gain stage, and output stage. It is set by bias voltage through the pass device. When the flipped voltage follower topology internally pushed two dominant poles, they are P_{gate} and P_{out} for stability purpose.

Generally analog circuit load needs an LDO with high power supply rejection (PSR), digital loads need fast transient response. Here LDO based on FVF single transistor based analog circuit load needs both high power

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supply rejection (PSR), and fast load transient response. So in this LDO based FVF internally setting to a lower value and heavy load conditions. It performs poor load regulation.

2.2. LDO Based on Flipped Voltage Follower with Inserted Buffer

Here buffer can be inserted between the gain stage and power stage of the single transistor based flipped voltage follower topology, because it provides a low input capacitance to VA and low output impedance to VG. I n the below fig.2 shows LDO circuit dominant poles are P_{out} and P_{gate} we should push into higher frequency. LDO based on FVF with inserted buffer consumes at light load conditions, and it helps pushing P_{gate} at stable load regulation .Another problem is occurred in output voltage of the low DC accuracy of V_{OUT}. So LDO based flipped voltage follower with inserted buffer circuit is stable load regulation perform.

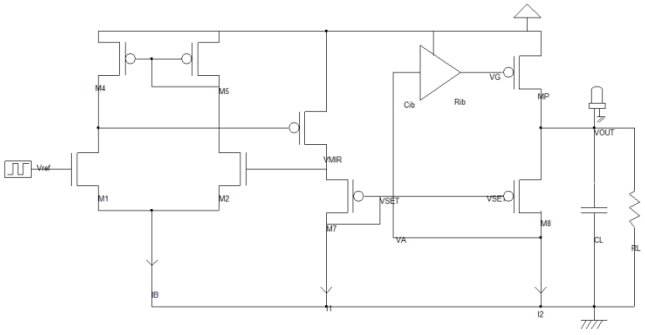

Fig.2 Schematic Diagram of LDO Based on Flipped Voltage Follower with Inserted Buffer

2.3 LDO Based on Three Loop Architecture

LDO based three loops architecture introduced using three inputs in the architecture .It can be improve DC accuracy, here using on chip capacitor for reduce gate leakage current. LDO based three loop architecture is achieve ultra-fast transient response and full spectrum power supply rejection. It is a high speed path, and in previous architectures only using two inputs , only V_{MIR} is generate V_{OUT} and V_{OUT} is not feed back to the error amplifier. But in this analysis error amplifier compares with V_{MIR} and reference voltage, V_{OUT} of the architecture. Here using three input transistors M1, M2, M3 are W/L ratios of (W/L)1: (W/L)2: (W/L)3=4:1:3 .So this ratios of transistors compared to VOUT that is represent

$$(V_{REF} - ¼\ V_{MIR} - ¾V_{OUT}) \times A_{EA} = V_{OUT} \qquad (1)$$

$$V_{MIR} = V_{OUT} + \Delta V \qquad (2)$$

Here EA is gain of the error amplifier, and ΔV is voltage difference between V_{MIR} and V_{OUT}, by substitute (2) into (1) and assume $A_{EA} >> 1$ and here

$$V_{OUT} = A_{EA}/1+A_{EA} \times V_{REF} - \frac{\Delta V.AEA/4}{1+AEA}$$

$$\approx V_{REF} - \Delta V/4 \qquad (3)$$

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$$V_{MIR} = A_{EA/1+}A_{EA}\times V_{REF} - \frac{\Delta V.AEA/4}{1+AEA} + \Delta V/1 + A_{EA}$$

$$\approx V_{REF} + 3\Delta V/4 \qquad (4)$$

So here V_{OUT} is closer to V_{REF} then V_{MIR} by the transistors ratios of M2 and M3 is 1:3.The LDO based three loops architecture shown in fig.3.

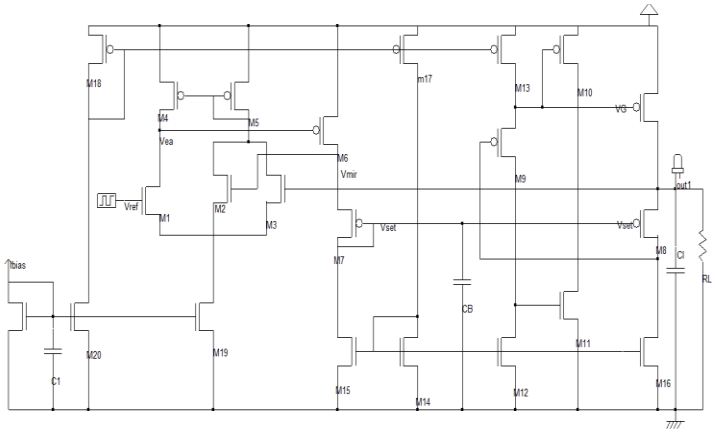

Fig. 3 Schematic diagram of LDO based on three loops architecture

2.4. LDO Based on Simplified Three Loop sarchitecture

Simplified three loop inputs are compared with previous architecture shown in the fig.4. Here using input of error amplifier is not a high speed path, the input transistors of error amplifier is using tail current mirror transistors are implemented. Here using on chip capacitors for reduce gate leakage current, and single transistor LDO based FVF is a fast response. V_{SET} is a low speed path it does not contain much current but buffer of the low impedance path needs more current.

The circuit design of a LDO with simplified architecture shown in fig.4.The load regulation of the performance is enhanced as the open loop gain, the topology and the biasing current of the buffer is designed to the frequency and the transient response of the system. Transient specifications tend to dominate the bias current demands of the buffer. The LDO regulators achieved a high frequency range (up to 10 MHZ).

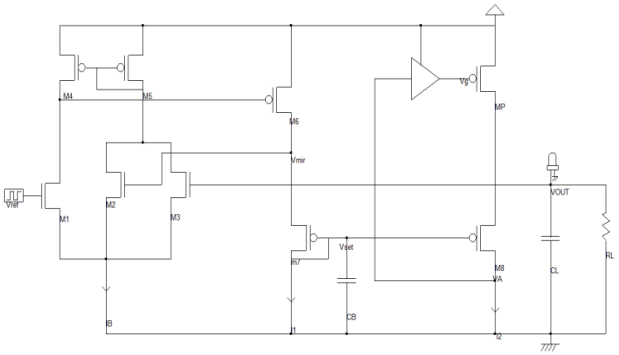

Fig. 4 Schematic Diagram of Simplified Three Loop Architecture

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III. DESIGN CONCEPT OF THE PROPOSED LOW-VOLTAGE LDO REGULATOR

3.1 Conceptual LDO based on Assistant push-pull output stage circuit

The proposed LDO regulator has been implemented by modifying the existing LDO based three loop architectures are ultralow-power dissipation is presented. This Low dropout regulator (LDO) using a class AB operational amplifier with assistant push-pull output stage (APPOS) circuit is to avoid external on chip capacitor while achieving fast regulation and is shown in fig.5.

To overcome those draw backs of existing methods, an LDO with an assistant push-pull output stage (APPOS) circuit is proposed. The APPOS circuit is serves as four main circuits that are overshoot detection circuit and under shoot detection circuits for detection of over deliver signals and under deliver signals. This type of circuits deliver an extra current, the below circuit represents optional low dropout regulator in which we are using capacitor inside the circuit. Because of capacitor are present in this circuit it takes more voltage drop inside it. Because of this reason it cannot deliver more energy to the circuits. The power consumption is more due to more dropping voltage inside the circuit.

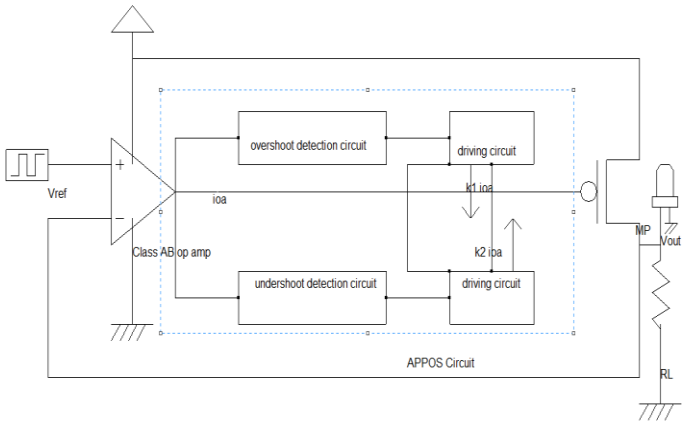

Fig.5 Schematic diagram of LDO based on APPOS circuit

3.2. Design LDO With The APPOS Proposed Circuit

A high loop gain is mandatory in LDO design to achieve optimum performance values such an accurate output that is line and load regulation and power supply rejection (PSR). A low supply voltage and output resistance reduction induced by limit the achievable gain of the class AB operational amplifier.Here using two cascade flipped voltage follower it acts as a level shifters for output stage of the class AB operational amplifier, and is shown in fig.6.

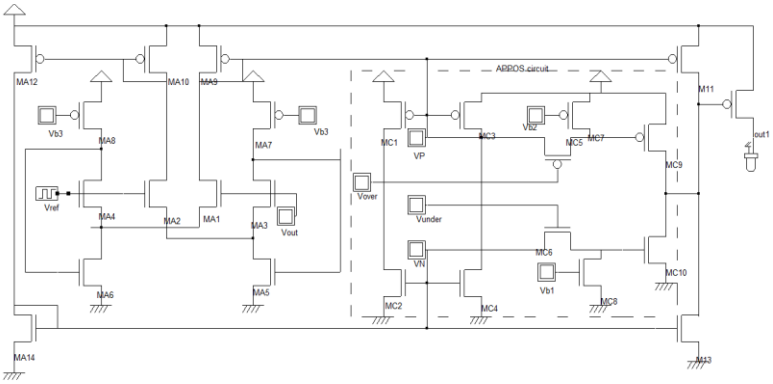

Fig.6 Schematic diagram of proposed LDO with the APPOS circuit

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The APPOS circuit can improve the slew rate while consuming very low bias currents for two complementary current sources. Hence the proposed LDO realized fast transient response with ultra-low power consumption.Transient analysis, and all schematic diagrams of simulation results shown in below section 4.

IV. SIMULATION RESULTS

Post layout simulations and comparisons are made for all these architectures where the proposed circuit has obtained much better dropout voltage when compared to the all existing schemes and the power consumption is slightly reduced. The simulations of the above all designs are carried out by using H-SPICE tool in CMOS technology. The simulated waveforms for all above circuits are shown in below.

4.1 Existing LDO

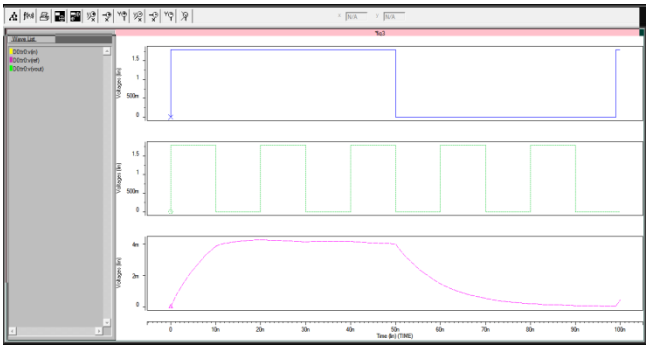

Fig.7 Simulation results for conventional LDO based on FVF topology

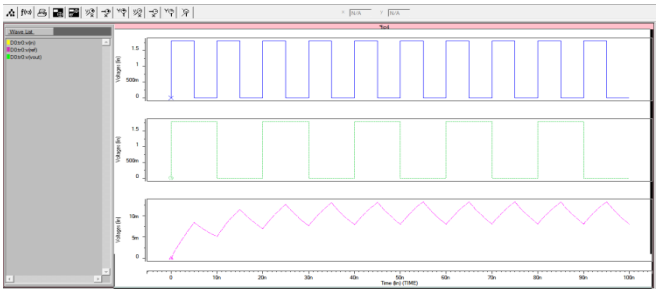

Fig.8 Simulation results for LDO based on FVF with inserted buffer

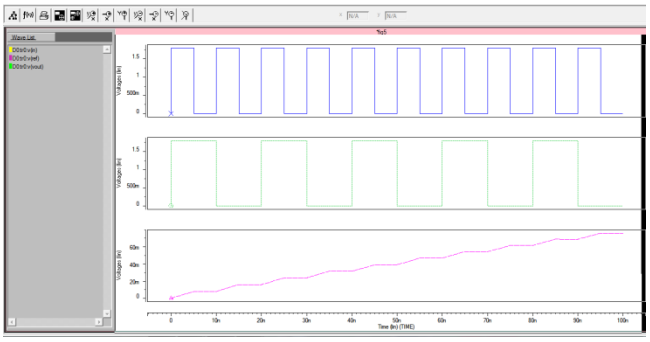

Fig.9 Simulation results for LDO based on three loop architecture

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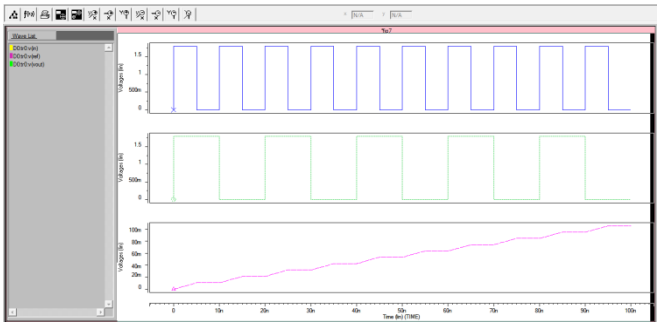

Fig.10 Simulation results for LDO based on simplified three loop architecture

4.2 Proposed LDO

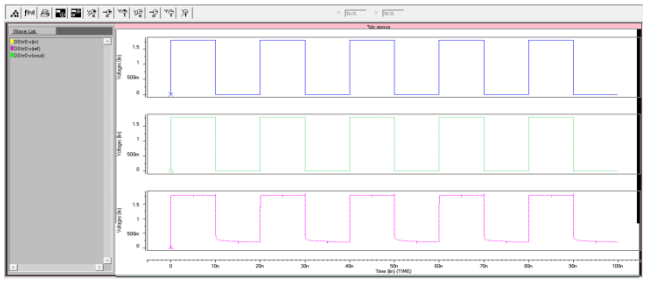

Fig.11 Simulation results of the proposed LDO with APPOS circuit

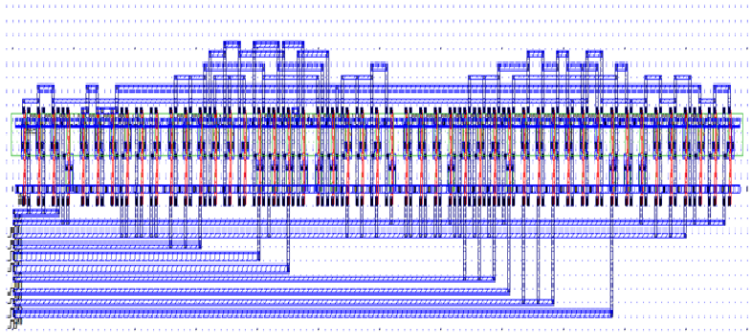

Fig.12 Layout of design LDO with the APPOS proposed circuit

TABLE1. PERFORMANCE COMPARISON

METHOD	VIN(V)	VDO(V)	POWER(W)
LDO on based flipped voltage follower	1.5V	1.496V	4.44949×10^{-5}
LDO based on FVF with inserted buffer	1.5V	1.485V	1.9200×10^{-4}

LDO based on three loop architecture	1.5V	1.42V	1.799×10^{-1}
LDO based on simplified three loop architecture	1.5V	1.4V	1.8706×10^{-4}
Proposed Design of LDO with APPOS circuit	1.5V	0.2V	1.3185×10^{-4}

Performance comparison table represents measured values of all the schemes are shown in table1 where reduce dropout voltage and power consumption is also reduced for the proposed LDO. The circuits presented in this work are analyzedby using the backend tool H-spice and designed in 180-nm technology.

V. CONCLUSION

An LDO Regulator using Assistant push-pull output stage circuit with class AB operational amplifier is presented in this paper. To design LDO with APPOS circuit and avoid external on chip capacitor while achieving accurate regulation and fast response. It has been tested experimentally and compared with the various schemes of LDO regulator. The experimental result shows the LDO regulates output voltage at 1.3V from 1.5V supply voltage. The measured result shows that it has achieved better performance both in terms of dropout voltage and power consumption.

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