International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

AN ALTERNATIVE DELAY INSENSITIVE PARADIGM FOR LOW POWER SYNCHRONOUS DIGITAL CIRCUITS

K. Sushma[1], J. Sudhakar[2]

[1]PG Student, [2] Professor & Head, Department of ECE

Vignan's Institute of Engineering for Women, Visakhapatnam, Andhra Pradesh (India)

ABSTRACT

The development of synchronous circuits currently dominates the semiconductor design industry. However, there are major drawbacks to the synchronous circuits (clocked approach), eventually increases the difficulty of clock distribution which consumes more power and difficult to reuse the design. Asynchronous circuit (clock-less design) is one of the best approaches to reduce all these drawbacks. The self-timed circuit operates with less power, less noise, less electro-magnetic interference and easy to reuse the design compared to the synchronous circuits. The clock-less circuit provides the best performance compared to the clocked approach circuit. In a digital system, the basic technique of asynchronous circuit is Null Convention Logic (NCL). The Null Convention Logic is a symbolically complete logic, which expresses a process completely in terms of logic itself. This paper represents an introduction of Null Convention Logic with data wavefronts, NCL framework, fundamentals of NCL (27 Threshold gates) and transistor level implementation of NCL threshold gates.

Keywords:Null Convention Logic, delay insensitivity, logic gates, input completeness, NCL registration.

I. INTRODUCTION

Asynchronous circuits, also called as clock-less circuits or self-timed circuits are a part of digital logic circuits which doesn't require any global clocks. In 1990's, clock-less circuits were developed. As VLSI technology enrolled the sub-micron meter/ nanometer era, self-timed circuits have many advantages compared with the clocked circuits such as low power consumption, low electromagnetic interference (EMI) and high robustness. Asynchronous circuits are assembled into two models: Bounded-delay and Delay insensitivity [1,2].

1.1 Bounded Delay Model

In this model, delays are bounded in both gates and wires. Delays are added to avoid the hazardous condition [3]. This leads to extensive timing analysis for the correct circuit operation.

1.2 Delay Insensitivity

In this model, delays are unbounded in both logic gates, interconnects, and in wires. But wire delays are less than the logic element delays with the component delays [4]. Delay insensitivity yields the timing analysis and provides average correct circuit operation rather than bounded delay and clocked approach [5].

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

II. NULL CONVENTION LOGIC

Null Convention Logic (NCL) is a basic developed technique for designing asynchronous circuits. NCL gates are preferable for special case of the logical operators or gates available in digital VLSI circuit design. NCL is a model of isochronic delay insensitivity i.e., the quasi delay insensitivity, the delay in the fanout is assumed to be same. NCL circuits can handle dual-rail or quad-rail to accomplish the delay insensitivity. A single bit dual-rail signal D consists of two wires, D^0 and D^1, which consists any value in the set {DATA0, DATA1, NULL} as shown in figure 1. The DATA0 state (D^0=1 and D^1=0) corresponds to a Boolean logic 0, the DATA1 state (D^0=0 and D^1=1) corresponds to a Boolean logic 1, and the NULL state (D^0=0 and D^1=0) corresponds to an empty set. If the two rails are asserted (D^0=1 and D^1=1), this state is defined as an illegal state [6,7].

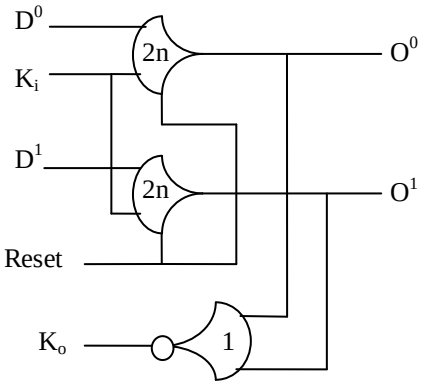

Figure 1: Single bit dual rail register

A single bit quad rail signal D consists of four wires, Q^0, Q^1, Q^2, Q^3, which consists any value from the set {DATA0, DATA1, DATA2, DATA3, NULL} as shown in figure 2. The DATA0 state (Q0=1, Q1=0, Q2=0, Q3=0) corresponds to two Boolean logic signals X=0 and Y=0. The DATA1 state (Q0=0, Q1=1, Q2=0, Q3=0) corresponds to X=0, Y=1. The DATA2 state (Q0=0, Q1=0, Q2=1, Q3=0) corresponds to X=1, Y=0. The DATA3 state (Q0=0, Q1=0, Q2=0, Q3=1) corresponds to X=1, Y=1. The NULL state (Q0=0, Q1=0, Q2=0, Q3=0) corresponds to an empty set. If the four rails are asserted (Q0=1, Q1=1, Q2=1, Q3=1) this state is defined as an illegal state.

2.1 Ncl Wavefront

A wavefront is the part of a DATA or NULL wavefront i.e., the request will be maintained with a same phase. A wavefront can't be overwritten with the opposite phase wavefront. The NULL wavefront is added to the DATA values (TRUE and FALSE) which represents the state of no data. The monotonic transitions are complete Null or complete Data [8].

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

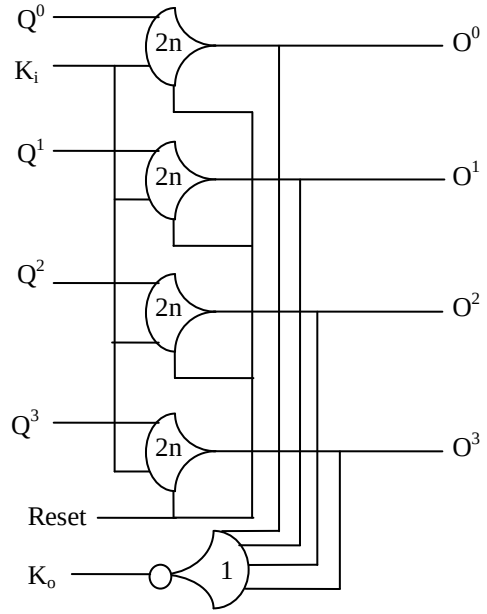

Figure 2: Single bit Quad Rail Register

The wavefront, transition from complete NULL to complete DATA is a Data wavefront, transition from complete DATA to complete NULL is a Null wavefront as shown in figure 3.

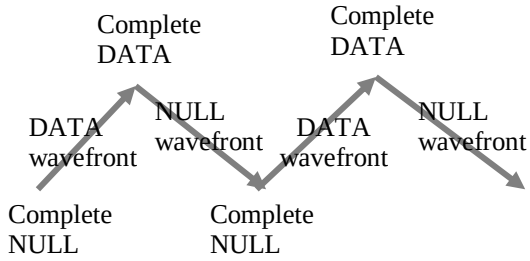

Figure 3: Wavefront Transitions

Consider a combinational circuit as shown in figure 4. Each number represents a Boolean gate. Assume that the initial state is Null condition, i.e., all input values and output values are Null.

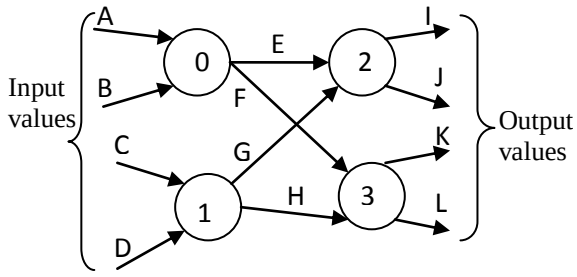

Figure 4: Example of Combinational circuit

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

If the input value is asserted that is A changes from Null to Data, but still output value remains Null state. The output value changes to Data, when gate 2 is asserted via E and F input values. Remaining K and L output values will be in Null state, until gate 3 is asserted via G,H input values. When all the output values are Data it means that complete set of input values are propagated to the circuit [8].

2.2 NCL Input Completeness

To achieve the input completeness of NCL circuit, all the inputs must be asserted. The output of a circuit will change from Null to Data, when all the inputs are transitioned to Data from Null and vice versa. In case of multiple outputs, some outputs get transitioned without input completeness, which results in more time consuming that is equivalent to the weak condition of delay insensitive [9].

2.3 NCL Observability

This is another condition, which provides the delay insensitivity for NCL circuits. An orphan may not be propagated through a gate. An orphan is defined as a wire that transitions during a current Data wavefront, but it's not determined at the output. Stability will ensure that every gate transition is observable at the output, which means that every gate transition is necessary to transit at least one output.

2.4 NCL Framework

The framework of NCL system is similar to the synchronous systems. This framework consists of the DI combinational circuit, which is inserted between the two DI registers. As shown in figure 5, it consists two DI registers, one DI combinational logic, two handshaking signals K_i and K_o via complete detection block. The register asserts signal K_o to request Data and de-assert it to request for Null. First Data sends by K_o to first DI register and sends to second DI register via DI combinational logic. The first DI register becomes empty (Null). While transferring the Data from the second DI register to further registers, then that register sends an acknowledgment that it does not contain any data and requests the previous DI register to send the next input through completion detection block [10].

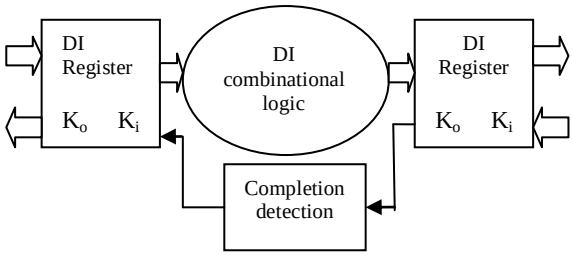

Figure 5: NCL system framework

2.5 NCL Registration

NCL circuit is a delay insensitive, because all the outputs will not be transitioned, until all the inputs are asserted. In this NCL registration, once the output of the register is Null, immediately it sends request for Data and vice versa. The purpose of NCL register is to store the data as per the output of NCL circuit and it is operated by the acknowledgement signals, i.e., request for Data (rfd) and request for Null (rfn). Assume the

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

NCL registration as shown in figure 6. This figure consists three NCL registers (Upstream, Current, Downstream) and NCL circuit is placed between the registers.

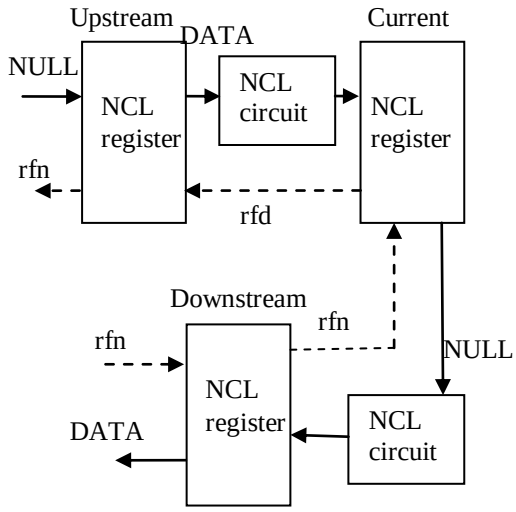

Figure 6: NCL registration

In NCL registration, upstream NCL register output is DATA, immediately it sends a handshaking signal rfn, i.e., request for NULL to previous register. Similarly, the current register output is NULL and sends an acknowledge signal rfd, i.e., request for DATA to upstream register and the downstream register output is DATA, it sends a handshaking signal rfn, i.e., request for Null to current register block [12]. This is the process of NCL registration.

2.6 NCL Logic Gate

The NCL threshold gate is completely differ from other delay insensitive pattern, which utilizes the state holding condition. The new technique of NCL delay insensitive, that was built with a hysteresis behavior [11]. The basic NCL threshold gate $TH_{mn,}$ where 1< m< n as shown in figure 7. A TH_{mn} gates have 'n' inputs and 'm' threshold value. The output of the threshold gate will be asserted, when 'm' of the 'n' input is asserted. As threshold gates follow the hysteresis design, all asserted inputs must be de-asserted before the outputs will be de-asserted. In the threshold gate $TH_{mn,}$ 'n' inputs are connected to the round portion of the gate and threshold value 'm' is written inside the gate[12,13].

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

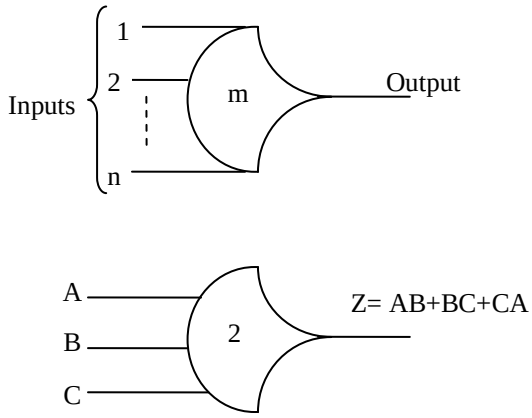

Figure 7: Threshold Gate th_{mn} and an Example th_{23}

Another type of threshold gate is a weighted threshold gate which is referred as $TH_{mn}W_{w1,w2,\ldots..wR}$ as shown in figure 8. Weighted threshold gate w_R is ranges between m and 1 i.e., $m > w_R > 1$ and R must be varies between 1 to n ($1 < R < n$). Consider, the threshold gate $TH_{34}W_{2,}$ where n=4 inputs which are labeled as A, B, C, D as shown in figure 8. The weight of input A, W(A) is 2 [14-16]. The threshold gate value is 3, so 3 of the 4 inputs must be asserted, then the output will be obtained as

$$Z = AB+AC+AD+BCD$$

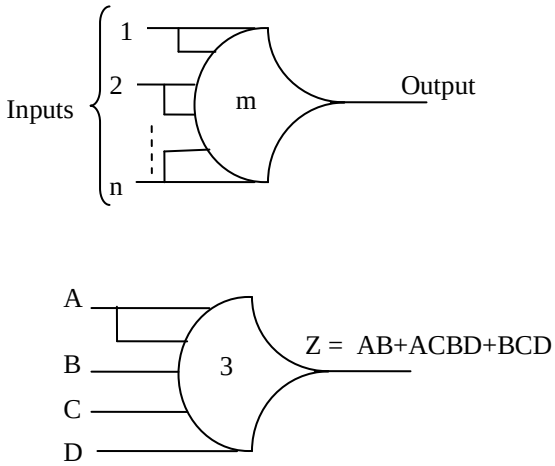

figure 8: weighted threshold gate $th_{mn}w_{w1w2\ldots wr}$ and an example of threshold gate $th_{34}w_2$

There are 27 fundamental threshold gates in NCL as shown in table 1. These gates are used to construct the NCL circuit with the Boolean equation. These gates have a four or fewer input variables.

III. IMPLEMENTATION OF NCL STANDARD THRESHOLD CELLS

Transistor level implementation of NCL logic gates was done with CMOS logic, which includes dynamic, semi-static and static implementation [15]. For each implementation, transistor count and performance levels will be increased with high speed and less time.

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

Table 1: NCL Threshold gates with their Boolean expressions

S.No.	NCL threshold gate	Boolean equation
1	TH12	A+B
2	TH22	AB
3	TH13	A+B+C
4	TH23	AB+AC+BC
5	TH33	ABC
6	TH23W2	A+BC
7	TH33W2	AB+AC
8	TH14	A+B+C+D
9	TH24	AB+AC+AD+BC+BD+CD
10	TH34	ABC+ABD+ACD+BCD
11	TH44	ABCD
12	TH24W2	A+BC+BD+CD
13	TH34W2	AB+AC+AD+BCD
14	TH44W2	ABC+ABD+ACD
15	TH34W3	A+BCD
16	TH44W3	AB+AC+AD
17	TH24W22	A+B+CD
18	TH34W22	AB+AC+AD+BC+BD
19	TH44W22	AB+ACD+BCD
20	TH54W22	ABC+ABD
21	TH34W32	A+BC+BD
22	TH54W32	AB+ACD
23	TH44W322	AB+AC+AD+BC
24	TH54W322	AB+AC+BCD
25	THXOR0	AB+CD
26	THAND0	AB+BC+AD
27	TH24COMP0	AC+BC+AD+BD

3.1 Dynamic Design Style

The basic building blocks of dynamic implementation are SET (NMOS transistors) and RESET (PMOS transistors) blocks as shown in figure 9. We can't say that this implementation is delay insensitive because delay insensitive follows hysteresis logic, but this implementation has no feedback. It mostly used in real time computer applications, but there is a minimum data guaranteed [15]. Dynamic logic circuits are not considered because they have higher switching dissipation, more gate leakage and high noise. To overcome this drawback, we consider a standard semi-static cell.

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

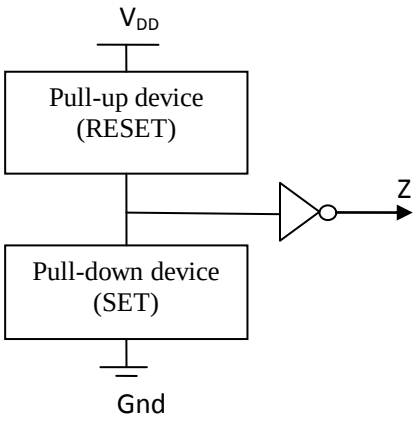

Figure 9: Dynamic implementation of NCL logic gate

3.2 Semi-Static Design Style

The semi-static design consist pull up network (RESET) and pull down network (SET) as shown in figure 10. A feedback inverter is placed to dynamic implementation block that is a weak feedback inverter to keep the charge on the internal node [15]. A weak inverter is used to follow the hysteresis logic. When neither of SET nor RESET is true, the weak inverter must be carefully sized. If the feedback inverter is not weak, then the reset block will not able to provide the current to feedback inverter and reset the output [17]. Another case, the feedback inverter will not provide sufficient current to prevent noise on the internal node. This drawback will be overcome in the standard static cell.

3.3 Static Design Style

NCL threshold gates are designed with hysteresis state holding functionality, i.e., after the output is asserted, all the input must be deasserted before the output is deasserted. To satisfy this process, additional PMOS transistors (HOLD0) and NMOS transistors (HOLD1) is placed instead of weak feedback inverter (semi-static implementation) as shown in figure 11 [16,17]. The HOLD0 and HOLD1 blocks are prescribed to keep the output value unchanged, when the SET and RESET functions are concealed as SET and RESET are complemented in NCL gates. The additional two blocks can be described as HOLD0=Z.$\overline{SET}$ and HOLD1=Z.$\overline{RESET}$.

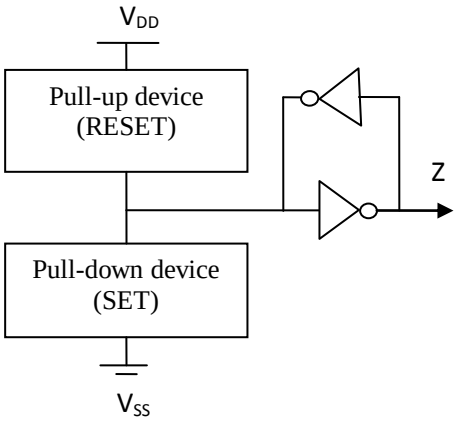

Figure 10: Semi-static implementation of NCL logic gate

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

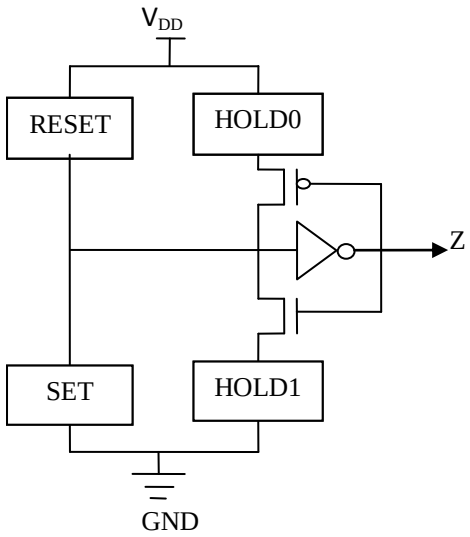

Figure 11: Static implementation

IV. IMPLEMENTATION OF NCL LOGIC OPERATIONS

The design of any circuit in NCL circuit is based on the Boolean expression. The optimization of NCL circuit can be done with the sum of product (SOP) expression [18-20].

4.1 OR Operation

General two input OR function expression is Z= X+Y. The canonical expression for $Z_0= X_0Y_0$ which can be summarized as TH_{22} gate. The canonical expression for $Z_1= X_1Y_1+X_0Y_1+X_1Y_0$ which can be summarized as $THand_0$ gate as shown in figure 12 and table 2 [18].

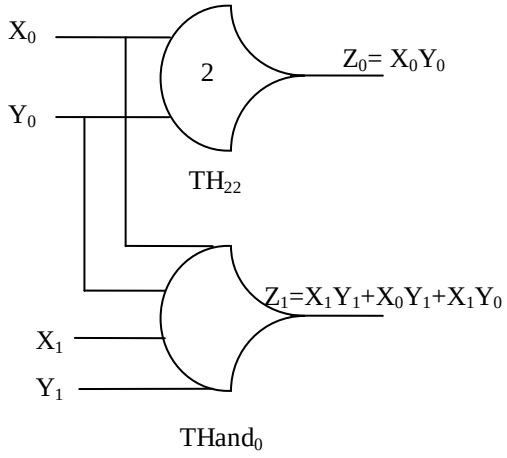

Figure 12: OR function in NCL

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

Table 2: Truth table- OR function in NCL

X_0	X_1	Y_0	Y_1	Z_0	Z_1
1	0	1	0	1	0
1	0	0	1	0	1
0	1	1	0	0	1
0	1	0	1	0	1

4.2 AND Function

The two input AND function expression is Z= XY. The canonical expression for $Z_0= X_0+Y_0$ which is summarized as TH_{12} gate. The canonical expression for $Z_1= X_1Y_1$ which can be summarized as TH_{22} gate as shown in figure 13 and table 3 [18,19].

Table 3: Truth table- AND function in NCL

X_0	X_1	Y_0	Y_1	Z_0	Z_1
1	0	1	0	1	0
1	0	0	1	1	0
0	1	1	0	1	0
0	1	0	1	0	1

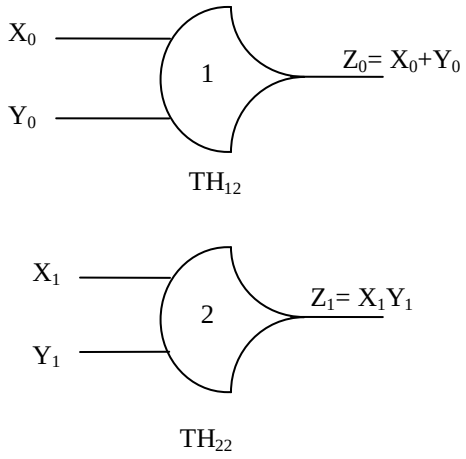

Figure 13: AND function in NCL

4.3 XOR Function

The two inputs XOR function expression is $Z= X^1Y+XY^1$. The canonical expression for $Z_0= X_0Y_0+X_1Y_1$ and $Z_1= X_0Y_1+X_1Y_0$ which is summarized as $TH_{24}comp_0$ gate as shown in figure 14 and table 4 [20].

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 02, July-December 2016
ISSN (O) 2321-2055
ISSN (P) 2321 -2045

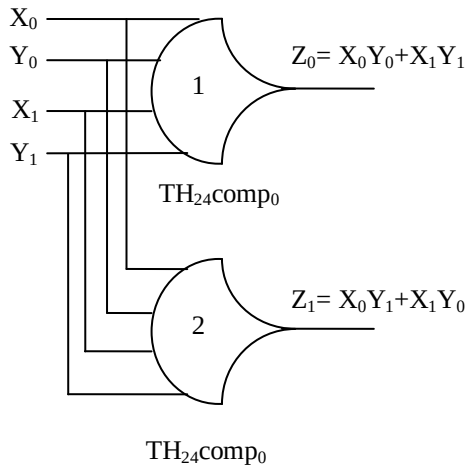

Figure 14: XOR function in NCL

Table 4: Truth table- XOR function in NCL

X_0	X_1	Y_0	Y_1	Z_0	Z_1
1	0	1	0	1	0
1	0	0	1	0	1
0	1	1	0	0	1
0	1	0	1	1	0

NCL circuits is one of the technique which belongs to completing an asynchronous circuit design.NCL doesn't depend on external sources such as clock, delay line or controller while processing [21,22]. It is completely expressed with high level languages without any need of timing issues.

Low cost due to the elimination of clock for any design and risks including clock skew. No need of any global clock, so the circuit can be designed in parts. It consumes power, at which the portion of the system is in working progress. With the combination of logic function and registration in single gate reduces power [22]. The NULL state in this NCL technique, power is in idle mode.

V. CONCLUSION

This paper deals with the advantages of asynchronous design, i.e., high speed, low power, less electromagnetic interference. The basic technique of the delay insensitive threshold network architecture is NULL Convention Logic, which holds the low power applications. Future extension of this work is to analyze the circuit performance to achieve high performance and ultra low power design requirements.

REFERENCES

[1] J.S.Yuan, "Teaching asynchronous design in Digital integrated circuits," Vol.47, pp.397, August 2004.

[2] J. Sparso and S. Furber.(December 2001, Principles of asynchronous circuit design- A systems perspective.

[3] A.J.Martin, "Programming in VLSI: from communicating processes to delay insensitive circuits."in developments in concurrency and communication, UT year or Programming Institute on Concurrent Programming, Addison-Welsey, 1990,pp.1-64.

[4] K. Van Berkel, "Beware the isochronic fork," Integration, the VLSI journal, Vol.13/2, pp.103-128,1992.

[5] Y.Kim and F.Lombardi, "Guest editors' Introduction: Clockless VLSI systems," IEEE design and test of computers: Special issue on Clockless VLSI design, Vol.30/6, pp. 26-36, November- December 2003.

[6] T.Verhoff, Delay insensitive codes. An overview,. Distibuted computing, Vol.3, pp. 1-8, 1998.

[7] J. Sudhakar, A. Mallikarjuna Prasad, Ajit Kumar Panda, "Multi Objective analysis of NCL threshold gates with Return to zero protocols," IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), Vol 10, issue 3, Ver. II (May- Jun 2015), PP12-17.

[8] K.M.Fant and S.A.Brandt, "NULL convention Logic: A complete and consistent logic for asynchronous digital circuits synthesis." Pp.261, 1996.

[9] C.L.Seitz, .System timing,. An introduction to VLSI systems, Addison Wesley, pp.218-262, 1980.

[10] S.C. Smith, R.F. DeMara, J.S. Yuan, M. Hagedorn, and D. Ferguson, "Delay insensitive gate level pipelining," Integration, the VLSI journal, Vol. 30/2 pp. 103-131, October 2001.

[11] Gerald E. Sobelman and Karl M. Fant, CMOS circuit design of threshold gates with hysteresis,. IEEE International symposium on circuits and systems (II), pp.61-65, 1998.

[12] J. Sudhakar, A. Mallikarjuna Prasad and Ajit Kumar Panda, "Behavior of Self Timed NCL circuits with Threshold variations", Intrnational Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages: 175-179 (2015).

[13] G. Vandana Devi, J. Sudhakar, "A study on Self Timed Approach for design of Low Power Circuits at Nanoscale", International Journal of Advances in Electrical and Electronics Engineering (IJAEEE), ISSN: 2319-1112/V4-N3-ICAESM: 216-220

[14] S.C. Smith, RF. DeMara, J.S. Yuan, D. Ferguson, and D. Lamb, "Optimization of NULL convention self-timed circuits," Integration, the VLSI journal, Vol.37/3, pp. 135-165, August 2004.

[15] S.C. Smith, "Completion- completeness for NULL convention digital circuits utilizing the bit-wise completion strategy," The 2003 International conference on VLSI, pp. 143-149, June 2003.

[16] Ortega, C.; Tse,J,; Manohar, R., "Static power reduction techniques for asynchronous circuits," Asynchronous circuits and systems (ASYNC), 2010 IEEE Symposium on, Vol., no., pp,52,61, 3-6 May 2010.

[17] Sankar, R.; Kadiyala, V.; Bonam, R.; Kumar, S.; Mohan, S.; Kacani, F.; Al-Assadi, W.K.; Smith, S.C., "Implementation of static and semi-static versions of a bit-wise pipelined dual rail NCL 2S complement multiplier," region % Technical Conference, 2007 IEEE, Vol., no., pp. 228,233, 20-22 April 2007.

[18] T.Y Wuu and S.B.K. Vrudhula, "A design of a fast and area efficient multi-input Muller C-element," IEEE Transactions on VLSI systems, Vol. 1, no.2, pp. 215-219, 1993.

[19] D.E. Muller, "Asynchronous logics and application to information processing," in switching theory in space technology, Stanford University press, 1963, pp. 289-297.

[20] M. Shams, J.C. Ebergen, and M.I. Elmasy, "Modeling and comparing CMOS implementations of the C-element," IEEE transactions on VLSI systems, Vol. 6, no. 4,pp. 563-567,1998.

[21] K.M. Fant, Logically Determined Design: Clockless system design with NULL convention logic., 1sted. Wiley-Interscience, 2005, pp. 292.

[22] E. Yahya and L.Fesquet, "Asynchronous design: A Promising paradigm for electronic circuits and systems." The 16th IEEE International Conference on Electronics, circuits and systems, p.339 (2009).