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A NOVEL ARCHITECTURE OF HIGH SPEED EXPONENTIAL BOOTH'S MULTIPLIER USING SQRT CSLA WITH BEC

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ABSTRACT
Multiplication is mostly used arithmetic operation that figures prominently in signal processing and scientific applications. Multiplication is a very hardware intensive subject and users are mostly concerned with getting low-power, smaller area and higher speed. There are many types of multiplier architectures present to perform the multiplication operation efficiently. For performing signed multiplication, the booth's multiplication algorithm is a powerful algorithm. Exponential numbers plays very important role in electronics, so there is need to develop circuits which can perform operations by using exponential numbers. In this paper, the design of 8-bit and 16-bit exponential Booth Multiplier using Square root carry select adder (SQRT CSLA) with Binary to Excess-1 Converter (BEC) is proposed. The proposed multiplier can be used to multiply exponential numbers. The real part of the exponential numbers are multiplied using booth's algorithm, where as the exponential part is added using SQRT CSLA with BEC. The proposed multiplier is compared with other exponential Booth's Multipliers which are designed using different adder architectures like Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Square root Carry select adder (SQRT CSLA) in terms of delay(ns) and area in terms number of LUTs occupied . All the multiplier architectures i.e., proposed and existing architectures are designed using VHDL and functionally simulated using Isim simulator. All the multiplier designs are to be synthesized using XST synthesizer.

Keywords: Booth's multiplier, Booth's algorithm, SQRT CSLA with BEC, VHDL, ISIM, Xilinx 14.2

1. INTRODUCTION

Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest clement in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel. Everyday new approaches are being developed to design low-power multipliers at technological, physical, circuit and logic levels. Several algorithms have been developed for this purpose like Booth's Algorithm, Wallace Tree method etc. The most powerful signed multiplication algorithm among all is Booth's multiplication algorithm. There are many types of numbers like real, complex, imaginary, exponential and so on. In electronics, frequently exponential numbers are encountered. So there is a need to develop circuits which

support the operations using exponential numbers. To perform exponential number multiplication, the real part of the exponential number is multiplied using any basic multiplication algorithm and the exponential part is added using adder. The exponential multiplier can act as an integral part in many digital electronic circuits; its speed decides the operation of that particular circuit.

To increase the speed of multiplication good and efficient multiplication algorithm must be chosen to design the exponential multiplier and also for the summation process several adder architectures are available. But to reduce the power consumption the summation architecture of the multiplier should be carefully chosen. By using Booth's multiplication algorithm [1],[2] and SQRT CSLA with BEC[3], an exponential Booth's multiplier architecture is proposed in this paper in order to achieve a high speed and area efficient multiplier architecture.

This paper in brief is structured as follows-section 2 describes about Booth's multiplication algorithm in brief. Section 3 describes about the structure and operation of SQRT CSLA with BEC. Section 4 describes about the exponential booth's multiplier design and operation using different adder topologies (RCA, CLA AND SQRT CSLA). Then section 5 explains in detail about the proposed exponential multiplier using SQRT CSLA with BEC. The implementation results of the proposed multiplier architecture and its comparison with the other exponential multipliers is presented in section 6. Finally this paper ends with conclusion.

II. BOOTH'S MULTIPLICATION ALGORITHM

The procedure to multiply two numbers using Booth's algorithm is as follows:

1. In given two numbers consider one as multiplicand and other as multiplier. Consider four registers A, B, Q_0 and Q_1, in which A, B and Q_0 registers are n-bit size where as Q_1 register is one bit size.
2. Initially, the registers A and Q_1 are set to 0 where as registers B and Q_0 are loaded with multiplicand and multiplier values respectively. Generally multiplication involves the operation of shifting and adding. To perform these operations, bits $Q_0(0)$ and Q_1 are scanned.
3. Depending on the values present in the $Q_0(0)$ and Q_1, the following operations are performed-

a. if $Q_0(0)$and Q_1 both have equal values i.e., 0-0 or 1-1, then all the bits of the A,Q_0 and Q_1 registers are shifted to right 1 bit.

b. If $Q_0(0)=0$ and $Q_1=1$ then the multiplicand value stored in register B is added with the current value of register A. After addition, all the bits of the A, Q_0 and Q_1 registers are shifted to right 1.

c. If $Q_0(0)=1$ and $Q_1=0$ then the multiplicand value stored in register B is subtracted with the current value of register A. After subtraction, all the bits of the A, Q_0 and Q_1 registers are shifted to right 1.

4. After the addition or subtraction, right shift occurs such that the leftmost bit of register A i.e., A_{n-1} is not only shifted into An-2, but also remains in An-1. This is required to preserve the sign of the number in A and Q_0 registers. It is known as arithmetic shift, since it preserves the sign bit. The value present in register A and Q_0 is the required product output of size 2n. Table 2.1 explains the operation to be performed depending on the bit values of $Q_0(0)$and Q_1.

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$Q_0(0)$	Q_1	OPERATION
0	0	Arithmetic shift right
0	1	Add multiplicand value with register A value and then Arithmetic shift right
1	0	Subtract multiplicand value with register A value and then Arithmetic shift right
1	1	Arithmetic shift right

Table 1 Operations to be performed depending on values $Q_0(0)$and Q_1

III. SQRT CSLA WITH BEC

There are many types of adder designs [4][7]. The Ripple Carry Adder (RCA) provides the most compact design but takes longer computing time. For an N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the RCA gives highest delay of all adders.

The Carry Look-Ahead Adder (CLA) gives fast results but consumes large area. For N≤4 CLA is fast, but for large values of N its delay increases more than other adders. So for higher number of bits, CLA gives more delay than other adders due to presence of large number of fan-in and a large number of logic gates. The Carry select adder (CSLA)[5] provides a compromise between RCA and CLA.

The CSLA is again of two types Linear CSLA (LCSLA) and SQRT CSLA. When both LCSLA and SQRT CSLA are compared in terms of speed, SQRT CSLA is faster. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers (mux). To reduce the area of SQRT CSLA the RCA with Cin=1 is replaced with BEC.As the SQRT CSLA is having less area and less delay when compared to other adder, it has been chosen as adder block in the proposed multiplier architecture.

3.1 Structure of SQRT CSLA with BEC

The SQRT CSLA with BEC is modified structure of basic SQRT CSLA. The basic SQRT CSLA consists of two RCA's (one RCA with CIN=0 and other RCA with CIN=1) due to which the area of adder is increased. To overcome this problem, the RCA with CIN=1 is replaced with BEC. The design of BEC consists less number of gates when compared with RCA. So the area of SQRT CSLA with BEC is less when compared to SQRT CSLA with dual RCA's. The structure of 8-bit SQRT CSLA with BEC is shown in fig 1. As shown in fig 1, the architecture of SQRT CSLA with BEC is obtained by replacing the RCA with C_{in}=1 with Binary-1 Converter (BEC) in the regular CSLA to achieve low area. The 8-bit SQRT CSLA with BEC can be divided into 3 groups. Group 1 consists of only a 2-bit RCA where as remaining groups i.e., group 2 and group 3 consists of a RCA with carry in 0, a BEC and a multiplexer.

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3.2 Operation of SQRT CSLA with BEC

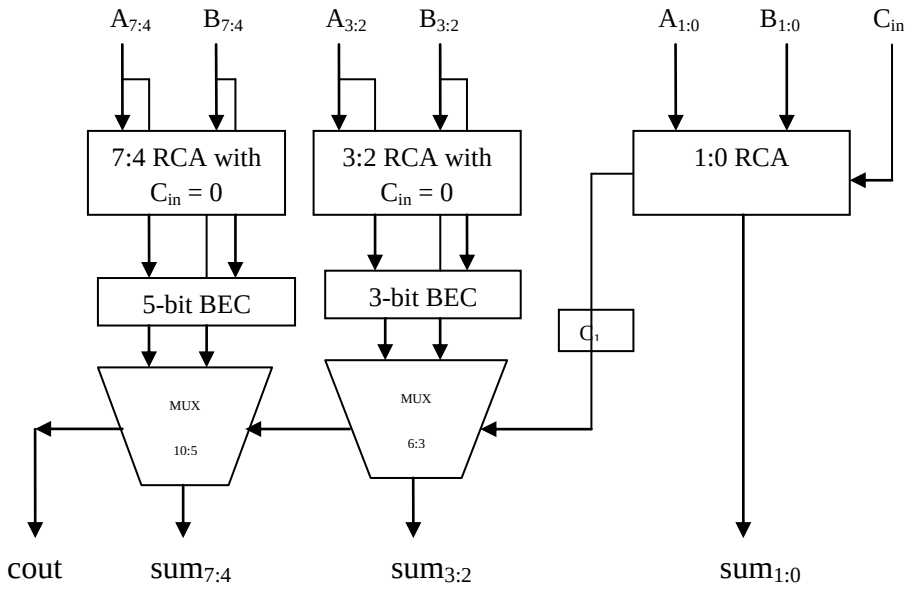

Figure 1 8-bit SQRT CSLA with BEC

The first group RCA performs addition operation on lower two bits with carry input. In group 2 and group 3, the RCA will perform addition operation and the output of the RCA is given as input to BEC. The operation of BEC is to add one to the input number. The output values of RCA and BEC are fed as input to multiplexer. The multiplexer is used to select the sum and carry values from the RCA and BEC by using the control signal to it. The control signal to multiplexer is nothing but the carry out of the previous group. If the control signal is 1 then sum and carry out of BEC is selected by the multiplexer and if control signal is 0 then sum and carry out of RCA with C_{in}=0 is selected by the multiplexer.

IV. EXPONENTIAL BOOTH'S MULTIPLIER USING DIFFERENT ADDER TOPOLOGIES (RCA, CLA AND SQRT CSLA)

4.1 Exponential Booth's multiplier using RCA

An exponential booth's multiplier design consists of an adder block. In the place of adder block one can use any type of the available adder design [6].Figure (2) shows the architecture of exponential Booth's multiplier using RCA. Its architecture has four registers, a Booth's multiplication algorithm block, one XOR gate and one RCA block.

In this the first register i.e., register A is used to store the multiplicand input value, second register i.e., register B is used to store the multiplier input value, third register i.e., register exponential B is used to store the exponential value of the multiplicand input and fourth register i.e., register exponential B is used to store the exponential value of multiplier input. Each register is having four inputs. They are CLK which is nothing but clock input, CLR is clear input which is used to clear the register contents, LD is load input used to load input values into the register and 8-bit input value. All the four registers are of 8-bit size. The Booth's multiplication algorithm is used to multiply the multiplicand with the multiplier. The 8-bit RCA block is used to add the exponent values of multiplicand and multiplier inputs.

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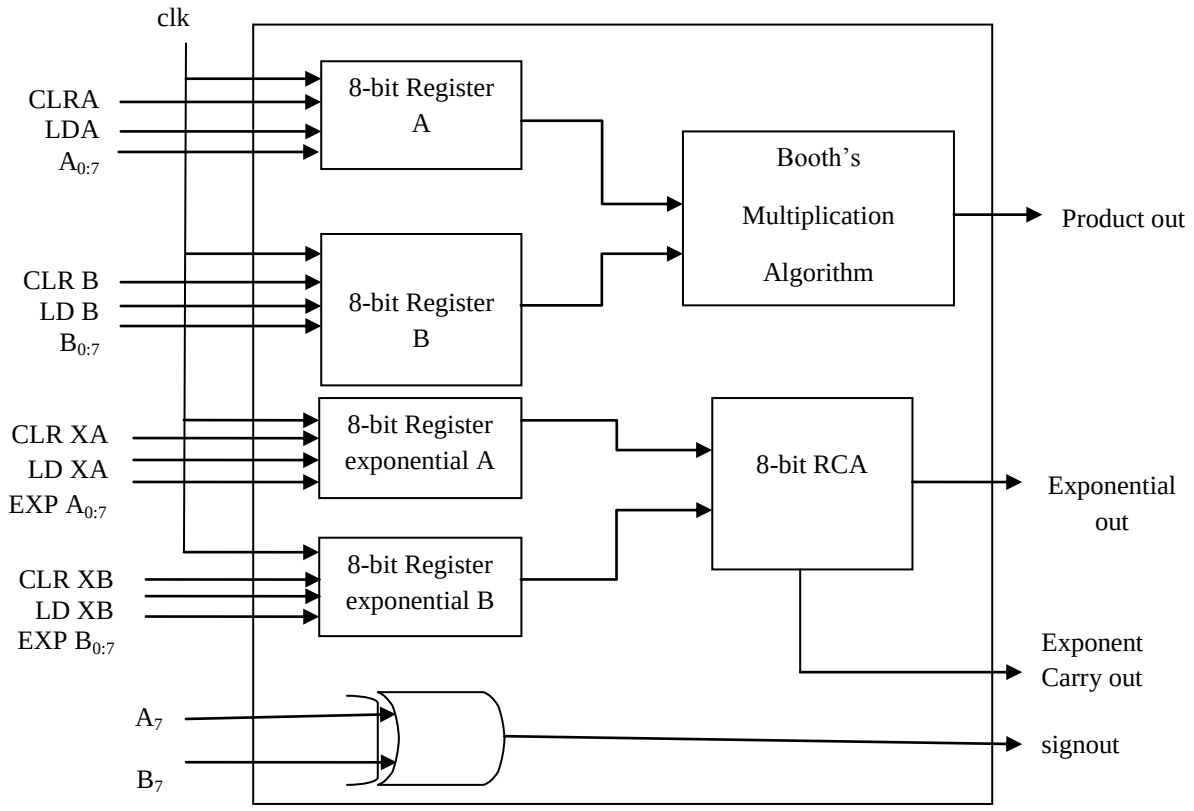

Figure 2 Exponential Booth's multiplier using RCA

The input to the multiplier is two 16-bit exponential numbers in which 8-bit is real part and 8-bit is exponential part. The input values are applied to respective registers. The output of register A and B are nothing but multiplicand and multiplier input values respectively which are applied to the Booth's algorithm block. The output of the Booth's algorithm is product output.

The input to the multiplier is two 16-bit exponential numbers in which 8-bit is real part and 8-bit is exponential part. The input values are applied to respective registers. The output of register A and B are nothing but multiplicand and multiplier input values respectively which are applied to the Booth's algorithm block. The output of the Booth's algorithm is product output.

The exponential values of the multiplicand and multiplier are added by using RCA and the output of adder is the exponential output. To find the sign of the output a XOR gate is used. The input to XOR gate is the MSB bits of the real part of input. The output of the XOR gate defines the sign of the output. The disadvantage of this structure is that as it is using a RCA block to perform addition of the exponents. The RCA operation will become slow as the number of input bits to it going to increase.

4.2 Exponential Booth's Multiplier using CLA

Figure (3) shows the architecture of exponential Booth's multiplier using CLA. The architecture and operation of this multiplier is same as explained in section 4.1 except the adder block used. In this multiplier, CLA is used to add the exponent values. The drawback of this architecture is the area of the adder increases with increase in number of input bits to it.

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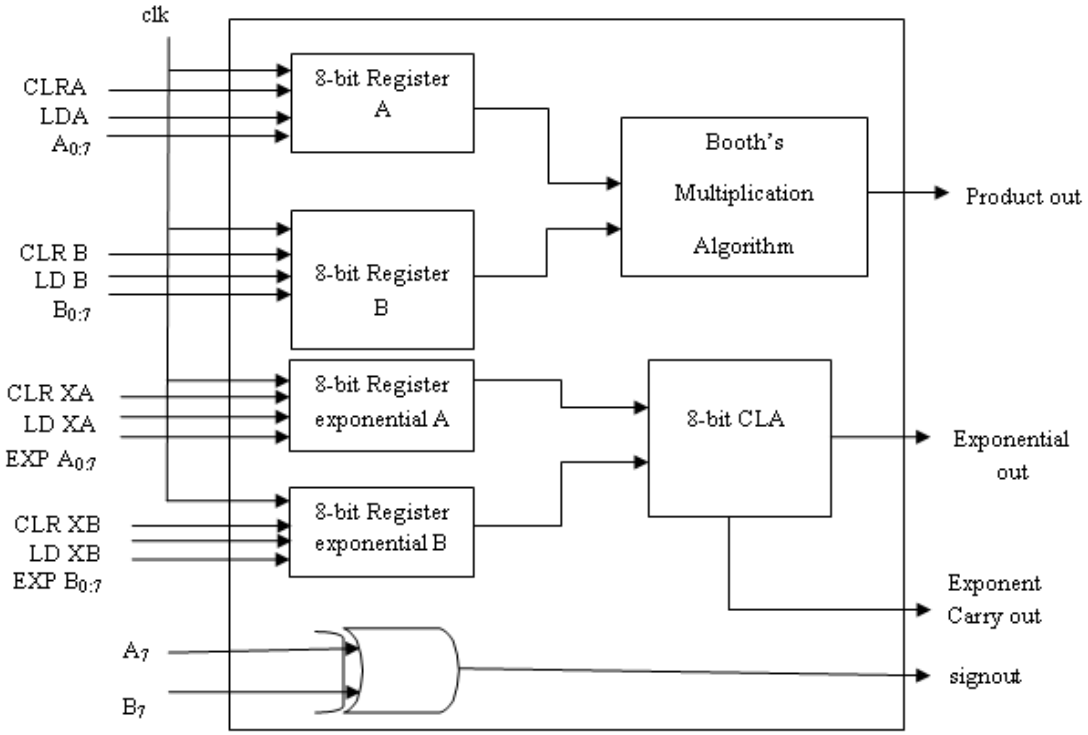

Figure 3 Exponential Booth's multiplier using CLA

4.3 Exponential Booth's Multiplier using SQRT CSLA

Figure (4) shows the architecture of exponential Booth's multiplier using SQRT CSLA. The architecture and operation of this multiplier is same as explained in section 4.1 except the adder block used. In this multiplier, SQRT CSLA is used to add the exponent values as shown in fig 3. The disadvantage of this structure is the area of the adder is more as the SQRT CSLA design consists of dual RCA's.

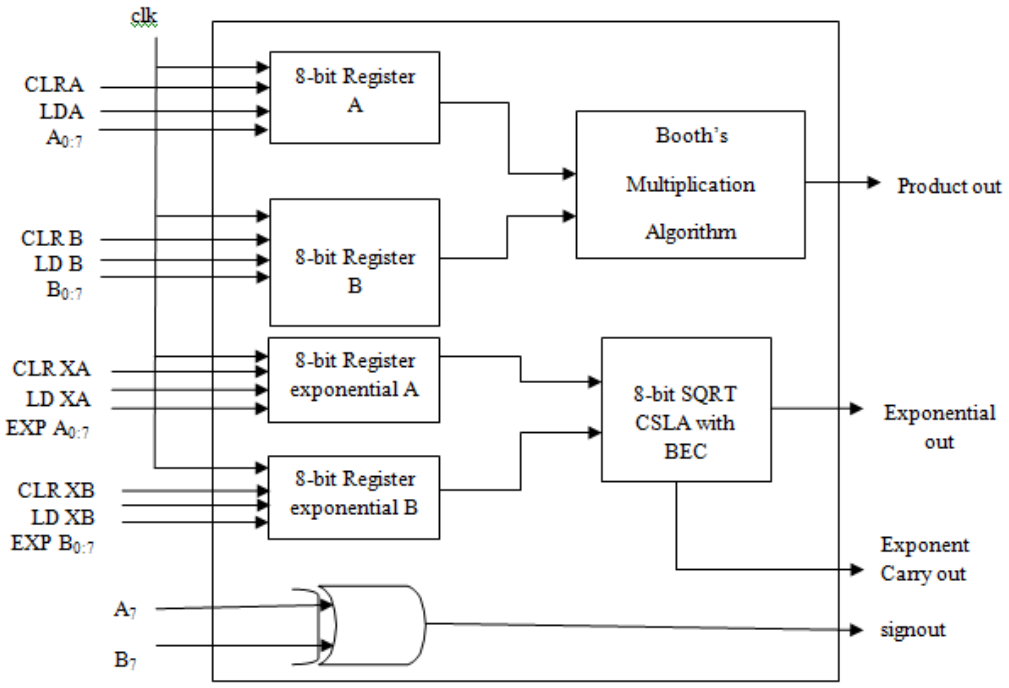

Figure 4 Exponential Booth's multiplier using SQRT CSLA

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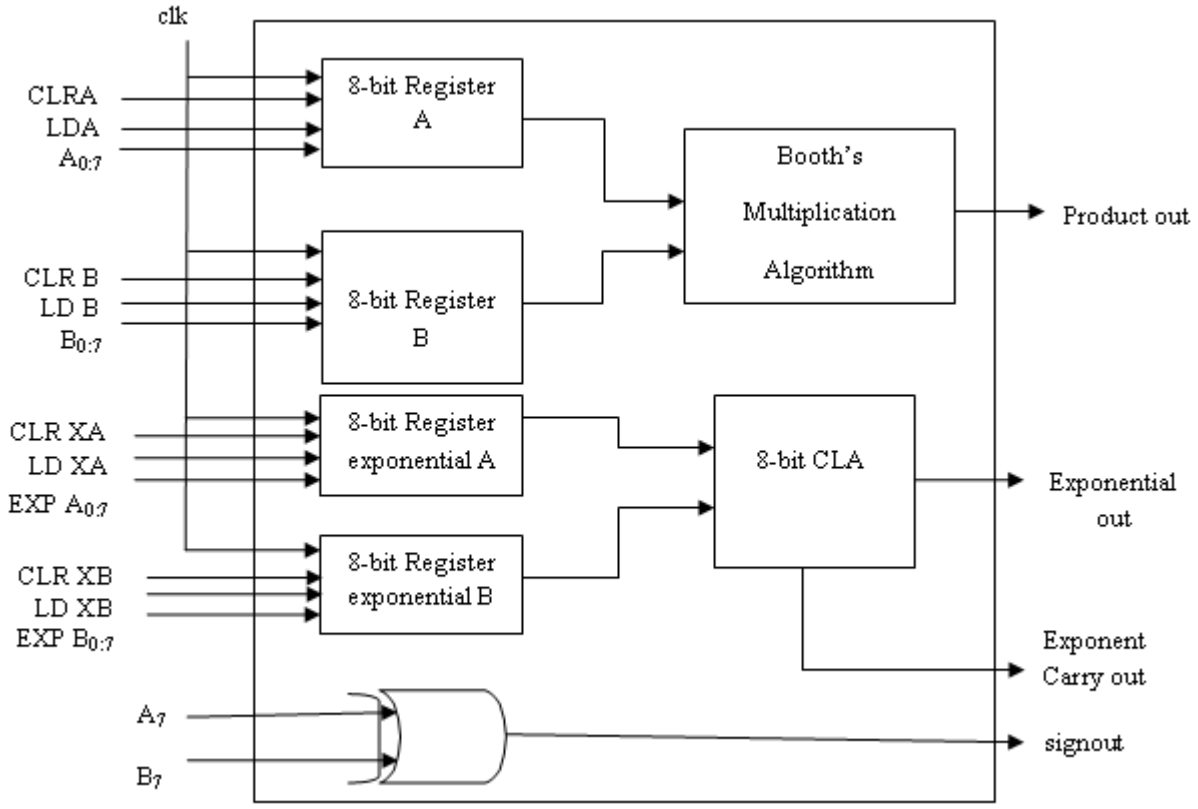

Figure 5 Exponential Booth's multiplier using SQRT CSLA with BEC

V. PROPOSED EXPONENTIAL BOOTH'S MULTIPLIER USING SQRT CSLA WITH BEC

This proposed multiplier mainly aims to overcome the drawbacks which were encountered in the previous designs. In this multiplier, SQRT CSLA with BEC is used as adder block. The advantage of this adder is explained in section 3.1. Figure 5 shows the architecture of exponential Booth's multiplier using SQRT CSLA with BEC. The architecture and operation of this multiplier is same as explained in section 4.1 except the adder block used. In this multiplier, SQRT CSLA with BEC is used to add the exponent values as shown in fig 5.

VI. RESULTS AND COMPARISON

The proposed exponential Booth's multiplier using SQRT CSLA with BEC is designed for 8 and 16 bit size using VHDL. Also three other multiplier architectures i.e., Exponential Booth's multiplier using RCA, Exponential Booth's multiplier using CLA and Exponential Booth's multiplier using SQRT CSLA are designed for 8 and 16 bit using VHDL in order to make comparison with the proposed multiplier architecture. Functional simulations are carried out by using Xilinx ISIM simulator. The multiplier designs are synthesized using a XST synthesizer. It is a synthesis tool from Xilinx. It provides area report and delay report of the design in terms of number of LUTs, slices occupied and in Nano seconds respectively.

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Input size	Multiplier type	Delay(ns)	Number of LUTs occupied
8-bit	Exponential Booth's multiplier using RCA	8.06	47
	Exponential Booth's multiplier using RCA	8.069	47
	Exponential Booth's multiplier using SQRT CSLA	8.121	45
	Exponential Booth's multiplier using SQRT CSLA with BEC	8.138	44
16-bit	Exponential Booth's multiplier using RCA	12.989	83
	Exponential Booth's multiplier using RCA	12.989	81
	Exponential Booth's multiplier using SQRT CSLA	10.923	80
	Exponential Booth's multiplier using SQRT CSLA with BEC	10.682	77

Table 1 Comparison of four multiplier architectures in terms of delay (ns)

From the above table 1, it is clear that the multiplier using SQRT CSLA with BEC is faster when compared with the other three multipliers. As shown in table 1, 16- bit exponential Booth's multiplier using SQRT CSLA with BEC has 10.682 ns delay to output the result where as the remaining has- Exponential Booth's multiplier using RCA has 12.989 ns, Exponential Booth's multiplier using CLA 12.989 ns and Exponential Booth's multiplier using SQRT CSLA has 10.923 ns delay to output the result. So it can be said that of all the designed multipliers, the proposed Exponential Booth's multiplier using SQRT CSLA with BEC is faster. Also the number of LUTs occupied by proposed multiplier is less when compared to others as shown in table 1.

VII. CONCLUSION

The proposed booth's multiplier is designed for 8-bit and 16-bit input size and it is compared with the other booth multipliers which are designed using Carry Adder (RCA), Carry Look Ahead Adder (CLA), Square root Carry select adder (SQRT CSLA). The Exponential Booth's multiplier using SQRT CSLA with BEC has minimum delay compared to other multiplier architectures and also occupied area is less than the multiplier architectures designed using RCA, CLA and SQRT CSLA. The 8-bit Exponential Booth's multiplier using SQRT CSLA with BEC is having the highest delay when compared to other multipliers. But, in the case of 16-bit multipliers Exponential Booth's multiplier using SQRT CSLA with BEC has the lowest delay i.e., 10.682 where as the Exponential Booth's multiplier using RCA and Exponential Booth's multiplier using CLA has a delay of 12.989 ns and Exponential Booth's multiplier using SQRT CSLA has 10.923 ns. So it can be concluded that as the number of input bits are going to increase the delay of the Exponential Booth's multiplier using SQRT CSLA with BEC is also going to be decreased. Exponential Booth's multiplier using SQRT CSLA with BEC is the best multiplier architecture compared to other designed multiplier architectures in terms of speed and also area. So it can be concluded that the Exponential Booth's multiplier using SQRT CSLA with BEC is having less delay and can be used for high speed application circuits.

REFRENCES

Journals

[1] "Booth's Multiplier: Ease of multiplication", Deepali Chandel, Gagan Kumawat, Pranay Lahoty, Vidhi Vart Chandrodaya , Shailendra Sharma; International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013

[2] "Design and Implementation of Booth's Multiplier and Its Application Using VHDL",Akanksha Sharma, Akriti Srivastava, Anchal Agarwal, Divya Rana ,Sonali Bansal, International Journal of Scientific Engineering and Technology (ISSN : 2277-1581) Volume No.3 Issue No.5, pp : 561-563 1 May 2014

[3] B. Ramkumar and Harish M Kittur , "*Low-Power and Area-Efficient Carry Select Adder*" IEEE transactions on very large scale integration (VLSI) systems, vol. 20, no. 2, February 2012., pp.340–344, 1962.

[4] R.UMA, VidyaVijayan, M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.

[5] O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput.

[6] "Performance Analysis of Modified Booth's Multiplier with use of Various Adders", Ms. Jasbir Kaur, Mandeep Singh, INTERNATIONAL JOURNAL OF SCIENTIFIC & ENGINEERING RESEARCH, VOLUME 4, ISSUE 6, MAY 2013 ISSN 2229-5518

Books

[7] J. M. Rabaey, Digtal Integrated Circuits—A Design Perspective. Upper Saddle River, NJ: Prentice-Hall, 2001.