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NOVEL APPROACH FOR MAC UNIT USING VEDIC MATHEMATICS

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ABSTRACT

This paper describes and compares the various approaches for designing of MAC unit. Various approaches for designing of MAC unit are Booth multiplier, modified Wallace multiplier and Vedic mathematics. In this among all sutras of Vedic mathematics Urdhva Tiryakbhyam sutra is used as it increases the speed of the system. Different types of addition algorithms are also discussed. The goal of this paper is to design a MAC unit which is comparable in speed.

Keywords: Booth Multiplier, Kogge Stone Adder, Modified Wallace Multiplier, Urdhva Tiryakbhyam, Vedic Mathematics.

I. INTRODUCTION

MAC unit plays a very essential role in many Digital Signal Processing applications such as fast fourier transform, filtering, discrete cosine transform, convolution etc, as it involves multiplication and accumulation operations. Hence there is need to design a very efficient MAC unit in which delay, power consumption and area are important factors kept in check. MAC unit reduces the load of CPU as it operates independently. It consists of multiplier unit whose output is then added to the accumulator unit using an adder unit. MAC unit designed should operate in high speed and consume less power and area. Delay in a system is generated due to long multiplication process and various adders in the addition unit.

II. MULTIPLY AND ACCUMULATE UNIT

MAC unit consist of multiplier unit whose inputs are fetched from memory location and then the partial product generated is added in the adder unit and output is generated in the form of sum and carry. Then the final result is generated by adding sum and carry. In this Parallel in Parallel out (PIPO) accumulator is used. The MAC operation can be expressed by this equation (i):

$$Z=A*B+Z$$

where the multiplier A and multiplicand B have n bits each and end Z has (2n+1) bits[1].

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The block diagram of MAC unit architecture is shown in figure (a):

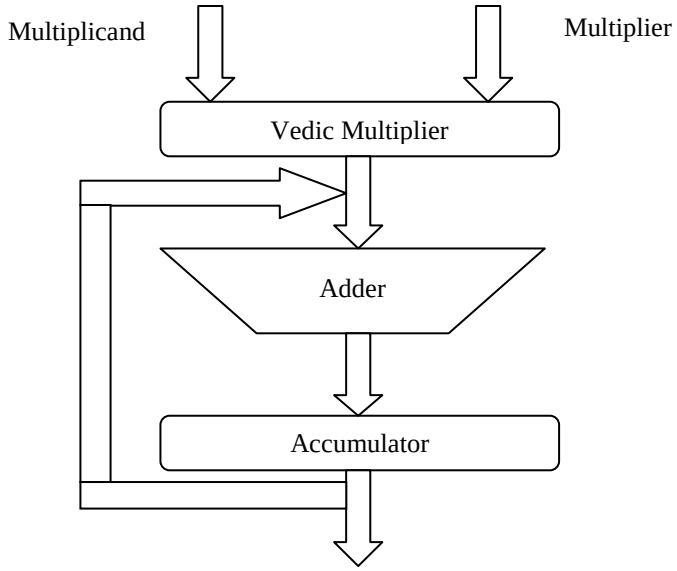

Figure a: Block Diagram of proposed MAC Unit Architecture

III. MULTIPLICATION ALGORITHMS

3.1 BOOTH WALLACE ALGORITHM

To accelerate the speed of multiplication Booth algorithm is used and carry select adder is used in adder stage with it. High speed multipliers are required as most of the DSP applications are dominated by multiplication stage. In this algorithm major bottlenecks are fast multiplication network and accumulator unit. The fast multiplication is dependent on three steps:

3.1.1 Partial Product Generation

In this Booth algorithm is used as with the generation of the partial product the speed of the system increases and the area decreases. The partial products generated are multiples of multiplicand and multiplier.

3.1.2 Partial Product Reduction

In this Wallace tree technique is applied which involves carry save adder for adding partial products as it is the fastest carry propagation adder.

3.1.3 Carry Propagation Adder

In this large size operands are added hence carry skip adder or carry select adder or carry look ahead adder is used.

Block diagram for Booth Wallace algorithm is shown in figure (b):

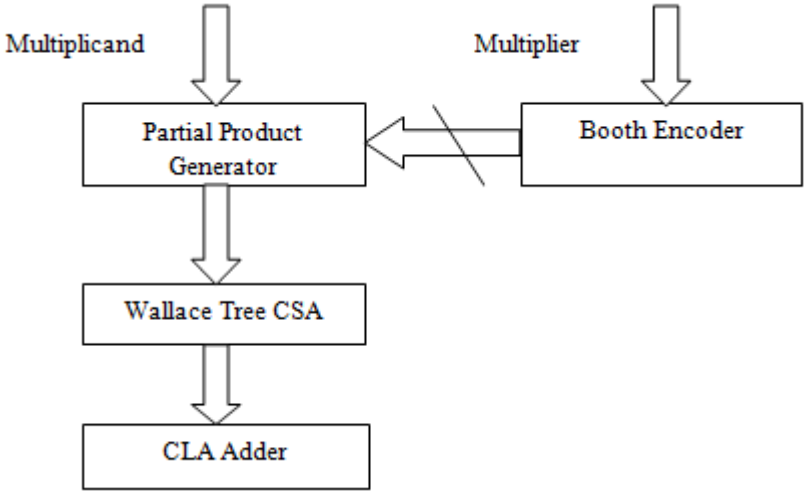

Figure b: Block Diagram of Booth Wallace Multiplier [4]

3.2 MODIFIED WALLACE ALGORITHM

In this algorithm a combination of modified Wallace multiplier and carry save adder is used to design the MAC unit. This technique is developed by using full adders and half adders for reduction stages. In this number of half adders are low as compared to the number of full adders in the system. A total of 10 stages are used in construction of a 64-bit modified Wallace multiplier.

3.3 VEDIC MATHEMATICS ALGORITHM

There are 16 sutras for multiplication but among all of them Urdhva Tiryakbhyam is used. This sutra is used to design multiplier unit as it reduces the partial product and increases the speed of the system.

3.3.1 Urdhva Tiryakbhyam Sutra

This sutra is also known as vertical and crosswise sutra as in this multiplication is done in this manner. This method is time, area and power economical. This increases the efficiency of the system and reduces the time delay. This method can be used for multiplication of decimal as well as binary numbers. In this multiplication first LSB of both digits is multiplied and the output generated is the LSB of sum. Then the LSB of first digit is multiplied with second number of the second digit and this output is added to the output of vice versa to obtain the second digit of the sum. Next the LSB of first digit is multiplied with MSB of second digit and vice versa then both the output values are added to the output generated from the multiplication of second number of both the digits. Then the MSB of both numbers is multiplied with each other to get the final product.

Diagrammatical demonstration of this multiplication is given in figure (c):

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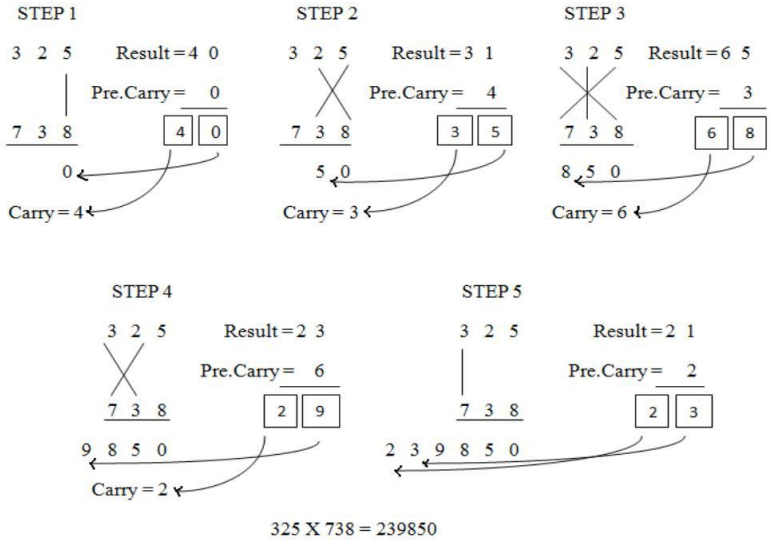

Figure c: Urdhva Tiryakbhyam Sutra Multiplication [4]

3.3.2 Vedic Multiplier

This technique of multiplication reduces the delay and number of stages of multiplication. In this N-bit streams can be divided into N/2=n bit length. This is much faster algorithm as compared to conventional algorithms. Block diagram of 32x32 bit multiplier is shown in figure (d):

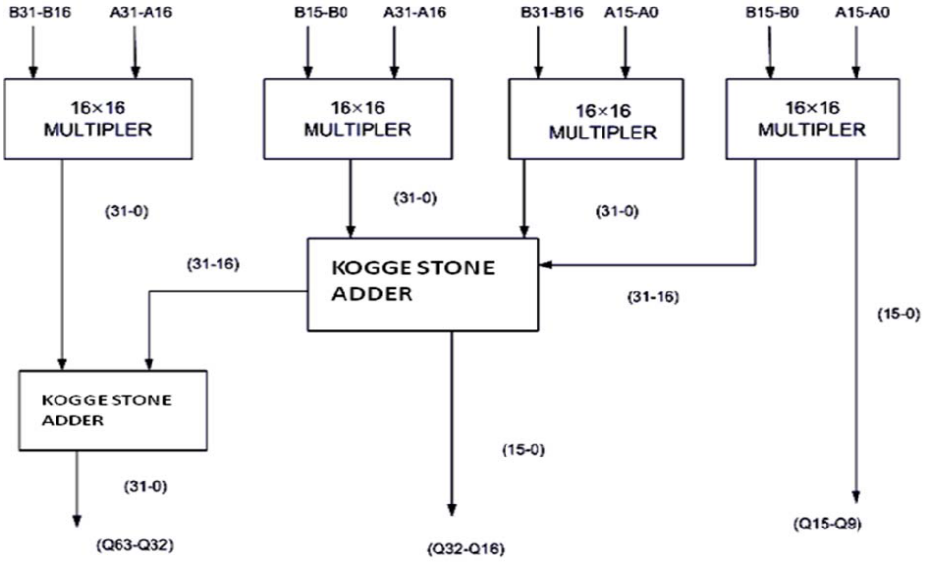

Figure d: Block diagram of 32x32 bit multiplier [2]

IV. ADDITION ALGORITHMS

4.1 Ripple Carry Adder

This consist of full adders and in this information is provided to first full adder which is then serially provided to other connected adder units until final sum and carry is generated. N bit ripple carry adder is shown in figure (e):

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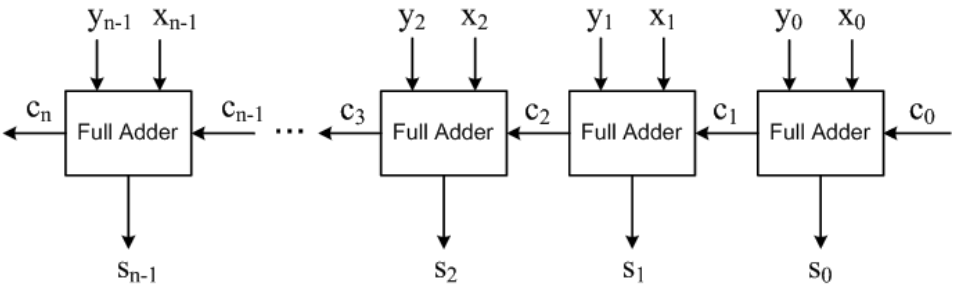

Figure e: Block diagram of Ripple Carry Adder [4]

4.2 CARRY LOOK AHEAD ADDER

In this type of adder it is determined that whether the given digits will generate carry or not. The carry is generated prior to the other outputs. In this type of adder carry generation, propagation and obliteration is the key factor. The general equation for the adder is given in equation (ii):

$$C_0 = A * B + (A \text{ xor } B)\ Cin$$

Diagrammatical representation of a carry look ahead adder is shown in figure (f):

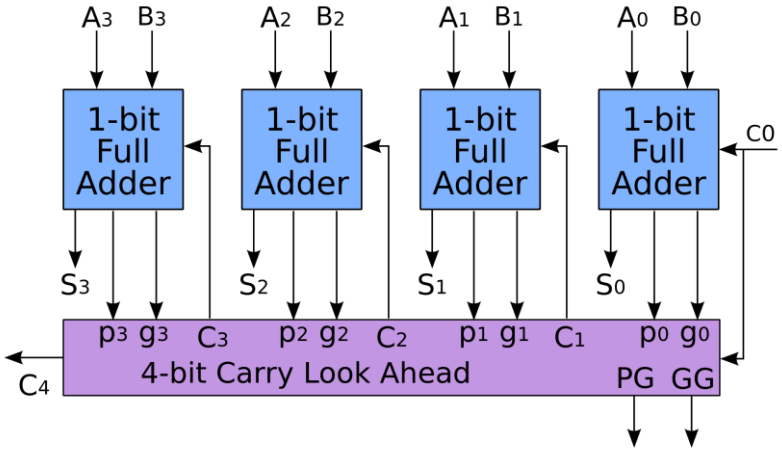

Figure f: Block diagram of Carry Look Ahead Adder [4]

4.3 Carry Save Adder

This adder is suitable for addition of more than 3-bits. In this full adder and half adder are used to complete the design. In this carry generated from the first stage is propagated to next stage of same row. This carry rippled to the next stage induces some delays hence to remove these carry generated is passed diagonally to the next stage. Block diagram of the adder is shown in figure (g):

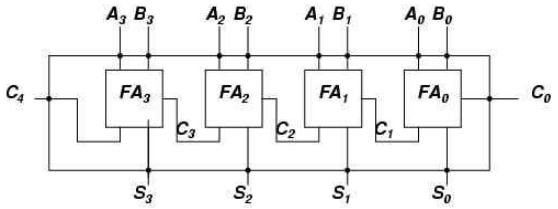

Figure g: Block diagram of Carry save Adder [4]

4.4 Kogge Stone Adder

This adder is a parallel prefix adder which is used to reduce power dissipation and is faster than rest of the adders. It is a form of carry look ahead adder. This adder has lowest fan out hence it increases the performance of the system. In this a bit is propagated and generated by each vertical stage. Carry bits are generated in last vertical stage and to generate the sum bits the carry bits are xor'd with initial propagated inputs.

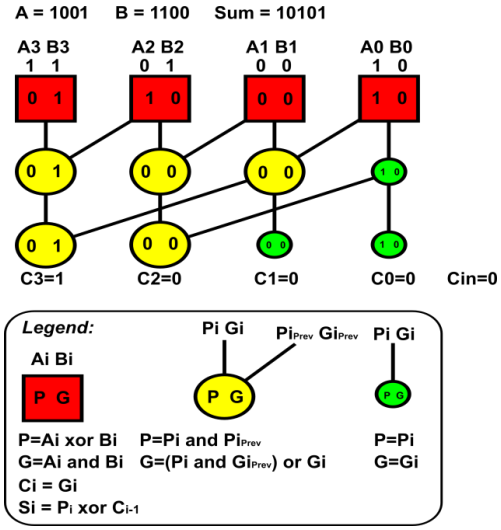

Figure h: Flow diagram of Kogge Stone Adder

V. ACCUMULATOR

It consists of adder and register, register is used to store the previous clock output from adder. This is implemented by using carry select adder or carry look ahead adder or carry skip adder. Adder and accumulator unit are firm foundation of MAC unit.

VI. CONCLUSION

It can be concluded that the design of MAC unit using Vedic multiplier (Urdhva Tiryakbhyam) and kogge stone adder is a better design as compared to others. The speed of MAC unit while using booth multiplier is 6.567 ns whereas while using booth Wallace multiplier is 6.436 ns and while using Vedic multiplier along with kogge stone adder is 4.932 ns. Hence the modified Vedic multiplier using kogge stone adder is the fastest thus making a better MAC unit design.

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