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QUALIFICATION OF IN-HOUSE DO-254 COMPLIANT DIGITAL SPEEDOMETER

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ABSTRACT

This paper describes prototype design of digital speedometer, identifying the components to miniaturized, miniaturization of digital components onto FPGA and Qualification of this modified approach of digital speedometer system. The digital speedometer is based on giant magneto resistance sensor. The digital speedometer system contains signal conditioning unit, processing unit and display unit. This approach is very laborious, manual and time consuming.

For schematic of digital speedometer is captured in Proteus design suite v8, digital components are miniaturized onto FPGA by writing functionality of digital components in Verilog. Simulation and Synthesis is done by using Xilinx software. And qualification is done by mapping the design project flow into DO-254 work flow. In advanced engineering process, tools play a very critical role. From requirements capture, design simulation, auto code generation and report generation tools are being used. So the output of these tools needs to be correct and complete. For safety critical systems, qualification is a must as the output of these tools are used to ensure the safety of the system being developed.

Keywords: FPGA, DO-254, Speedometer,

I. INTRODUCTION

In house embedded system is a digital speedometer used to measure and display speed of the automotive system in terms of rotations per minute (RPM). GMR sensor (Giant magneto resistance) can be used to sense the speed. Signal conditioning unit consists of operational amplifier and Schmitt trigger. Operational amplifier used to amplify the signal coming from the GMR sensor and Schmitt trigger is used to generate the pulses.

The dimension of this embedded is required to miniaturize. There is a need to miniaturize to design without effecting the functionality and performance. Re-designing the system in FPGA is one of the most preferred and proven approach.

Field programmable gate arrays are semiconductor devices that are based around the matrix of configurable logic blocks (CLB's) connected via programmable interconnects. FPGA's can be reprogrammed to desired applications or functionality requirements after manufacturing. Due to their programmable nature, FPGA's are ideal fit for many different markets. FPGA's can be used in many applications such as aerospace and defense, automotive, consumer electronics, broadcast, medical and wireless communications etc.

The verification of complex FPGA designs is becoming increasingly challenging for safety-critical applications within many sectors – such as aerospace, automotive and medical – and for mission-critical applications within

the defense sector. Also, verification must be inherent throughout the entire development lifecycle, from requirements specification to final hardware.

FPGA implementation is typically verified through RTL simulation, to validate design intent, and code coverage analysis to ensure 100% coverage of all possible input signal combinations across a series of applied tests.

However, while simulation results can be easily visualized, analyzed, compared and requirements traceability easily maintained, the design behavior in real hardware cannot be easily traced back to simulation because it is simply not possible to achieve 100% specification coverage once the FPGA is physically mounted onto a circuit board. Industry standards also provide guidelines to verify and validated the complex hardware designed using FPGA. RTCA DO-254 is one such approach which is widely being used in the safety critical aerospace applications.

This presents quite a problem in light of industry standard DO-254 (Design Assurance Guidance for Airborne Electronic Hardware) which requires that safety- and mission-critical designs be verified on the real hardware for certification purposes.

Hardware verification tends to be performed at the board-level; and the FPGA will probably contain most of the board's primary functions (certainly the time-critical ones). The FPGA will also typically connect with a host of other board-mounted components such as micros, DSPs and memory. To have full traceability you need to be able to compare the behavior of the physical outputs of the device with their corresponding RTL simulation results. However, you seldom if ever have a means of physically driving the hardware with all combinations of stimuli (as per the ones used for code coverage within your RTL simulation); and even for the inputs you can drive the creation of test vectors is an intensive, time-consuming manual task.

II. PROJECT OVERVIEW

In this approach the embedded system used is digital speedometer (tachometer) based on indigenously developed GMR sensors. The embedded system is used to measure the speed of the motor or vehicle used in automotive or aerospace applications.

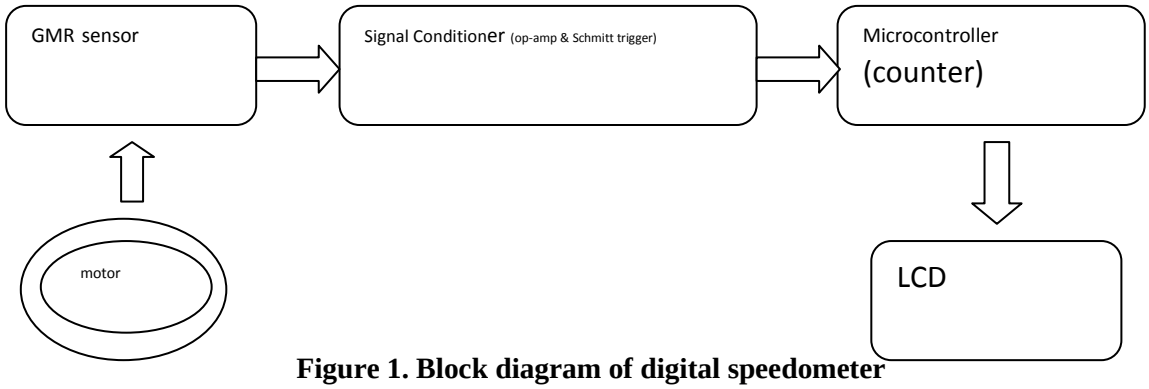

Figure 1. Block diagram of digital speedometer

Figure 1. Shows the block diagram of digital speedometer. It consists of the GMR sensor, signal conditioning unit, microcontroller used for counting the pulses and calculation of rotation per minute and display unit.

The research problem is to miniaturize the design.

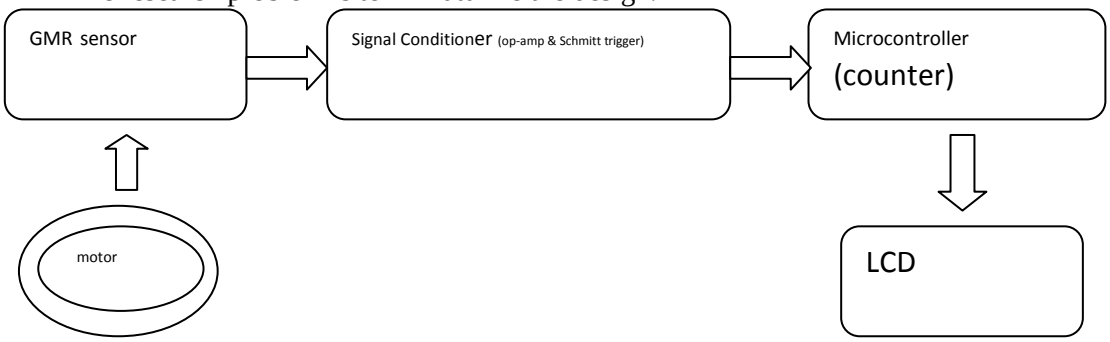

Figure 2. Block diagram of digital speedometer with highlighted portion

The highlighted portion in the figure 2 needs to be miniaturized to reduce the overall size of the system. Miniaturization is done by implementing the digital blocks onto the FPGA.

III. HALL EFFECT SENSOR

A Hall Effect sensor [14] is a transducer that varies its output voltage in response to a magnetic field. Hall Effect sensors are used for proximity switching, positioning, speed detection, and current sensing applications. In its simplest form, the sensor operates as an analogue transducer, directly returning a voltage. With a known magnetic field, its distance from the Hall plate can be determined. Using groups of sensors, the relative position of the magnet can be deduced.

Electricity carried through a conductor will produce a magnetic field that varies with current, and a Hall sensor can be used to measure the current without interrupting the circuit. Typically, the sensor is integrated with a wound core or permanent magnet that surrounds the conductor to be measured.

Frequently, a Hall sensor is combined with circuitry that allows the device to act in a digital (on/off) mode, and may be called a switch in this configuration. Commonly seen in industrial applications such as the pictured pneumatic cylinder, they are also used in consumer equipment; for example some computer printers use them to detect missing paper and open covers. When high reliability is required, they are used in keyboards.

IV. THE QUANTUM MECHANICS OF GMR

To understand how GMR works on the atomic level, consider the following analogies: If a person throws a ball (analogous to a conduction electron) between two sets of rollers turning the same direction (analogous to parallel spin-aligned magnetic layers), the ball tends to go through smoothly. But if the top and bottom rollers turn in opposite directions, the ball tends to bounce and scatter. Alternatively, the GMR effect may be compared to light passing through polarizers. When the polarizers are aligned, light passes through; when their optical axes are rotated with respect to each other, light is blocked [14].

The resistance of metals depends on the mean free path of their conduction electrons, which, in GMR devices, depends on the spin orientation. In ferromagnetic materials, conduction electrons either spin up when their spin is parallel to the magnetic moment of the ferromagnets, or spin down when they are antiparallel. In nonmagnetic conductors, there are equal numbers of spin-up and spin-down electrons in all energy bands. Because of the

ferromagnetic exchange interaction, there is a difference between the number of spin-up and spin-down electrons in the conduction bands. Quantum mechanics dictates that the probability of an electron being scattered when it passes into a ferromagnetic conductor depends on the direction of its spin. In general, electrons with a spin aligned with the majority of spins in the ferromagnets will travel further without being scattered.

In a GMR spintronic device, the first magnetic layer polarizes the electron spins. The second layer scatters the spins strongly if its moment is not aligned with the polarizer's moment. If the second layer's moment is aligned, it allows the spins to pass. The resistance therefore changes depending on whether the moments of the magnetic layers are parallel (low resistance) or antiparallel (high resistance).

Optimal layer thicknesses enhance magnetic-layer antiparallel coupling, which is necessary to keep the sensor in the high-resistance state when no field is applied. When an external field overcomes the antiparallel coupling, the moments in the magnetic layers align and reduce the resistance. If the layers are not the proper thickness, however, the coupling mechanism can destroy the GMR effect by causing ferromagnetic coupling between the magnetic layers. For spin-dependent scattering to be a significant part of the total resistance, the layers must be thinner (to a magnitude of several nanometres) than the mean free path of electrons in most spintronic materials. A typical GMR medical sensor has a conducting layer approximately 3 nm (or one ten-millionth of an inch) thick. For reference, that is less than 10 atomic layers of copper, and less than one ten-thousandth the thickness of a piece of tissue paper.

Benefits:	GMR	HALL	AMR
Physical Size	Small	Small	Large
Signal Level	Large	Small	Medium
Sensitivity	High	Low	High
Temperature Stability	High	Low	Medium
Power Consumption	Low	Low	High
Cost	Low	Low	High

Table 2 comparisons of different sensors with GMR

A. Sensors specification

For the development of speedometer unit, we have used GMR based sensors manufactured by Non – volatile electronics Inc. The pattern design of the sensor is similar to Wheatstone bridge this gives the differential output in the presence of the magnetic field. The output voltage is directly proportional to the magnitude of the field gradient i.e. dB/dX. Here dX is the distance between two sensing elements.

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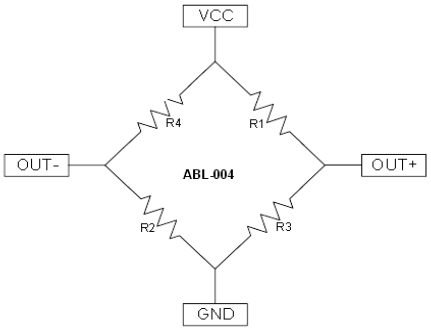

Figure 3. GMR (ABL-004) internal diagram

The key features are:

- Single bridge resistance R , min value is 4kΩ and max value is 7kΩ
- The operating voltage range is <1 V to 30V
- Maximum sensor sensitivity is 0.04% /Oe (1000 Oerstds = 1 guass)
- Saturation field range is -180 to +180 Oe
- Operating temperature range is -65 to 170

Differential sensors, or gradiometers, provide an output signal by sensing the gradient of the magnetic field across the sensor IC. For example, a typical GMR sensor of this type will have four resistive sensor elements on the IC, two on the left side of the IC, and two on the right. These resistive sensor elements will be wired together in a Wheatstone bridge configuration. When a magnetic field approaches the sensor IC from the right, the right two resistive sensor elements will decrease in resistance before the elements on the left. This leads to an imbalance condition in the bridge, providing a signal output from the bridge terminals.

V. PROTOTYPE DESIGN OF SYSTEM

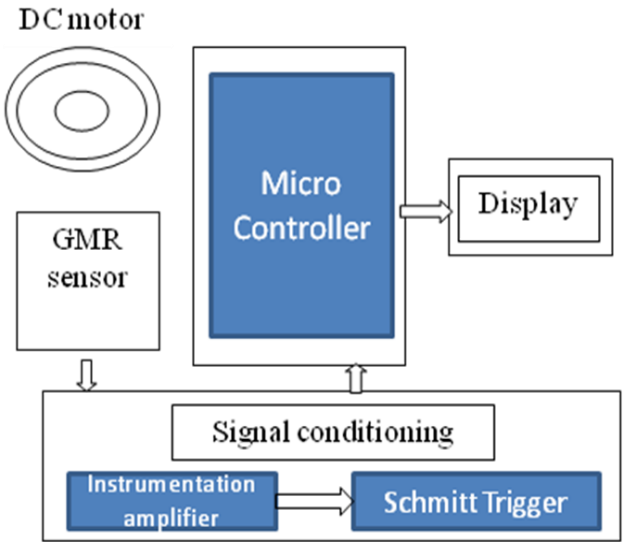

Figure 4. Block diagram of In house embedded system

Figure 4 shows hardware components for reference design of the digital speedometer which is designed in NAL. The system contains GMR sensor, Signal conditioning unit, controller unit and display unit. GMR sensor gives differential output signal on application of external field. Signal conditioning unit consists of instrumentation

amplifier used to amplify the signal coming from GMR sensor to 5V and Schmitt trigger is used generate the pulses. Microcontroller is used to count the pulses and display unit displays the speed.

VI. METHODS FOR CALCULATION OF THE SPEED

The signal coming from the GMR sensor is amplified using operational amplifier and converted into pulses using Schmitt trigger, these signals are given to the microcontroller for further calculation. The calculation includes two different methods.

A. Method 1

The first method is based on measuring the elapsed time between two successive pulses. The time elapsed between two successive pulses is to be counted, the obtained value time_count used in equation (5). The constant value from equation (5) was obtained considering that the GMR sensor used for these experiments gives N pulses/rotation and the sample rate was selected to be equal with FPGA working frequency (1MHz). Here we choose N=1

$$F_{cod} = N \times \frac{V_{RPM}}{60} \quad (1)$$

$$T_{cod} = \frac{60}{N \times V_{RPM}} \quad (2)$$

$$time\_count = \frac{T_{cod}}{T_{FPGA}} = \frac{60}{N \times V_{RPM}} \times \frac{1}{1 \times 10^{-6}} \quad (3)$$

$$const = \frac{60}{1} \times \frac{1}{1 \times 10^{-6}} = 60 \times 10^{6} \quad (4)$$

$$V_{RPM} = \frac{600000}{time\_count} \quad (5)$$

Where:

- Fcod – the frequency of the signal from the optical encoder;
- Tcod – the period of time of the signal from the optical encoder;
- time_count – the counted time elapsed between two successive pulses;
- TFPGA – FPGA working frequency, 20x10-9 s;
- Vrpm – the speed of motor, measured in rpm.

B. Method 2

The second method is based on constant elapsed time (CET) method. It consists in pulses counting during an established period of time. Say established time is 1sec. In this method, there are 16 pulses in one complete revolution of the motor.

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VII. HARDWARE DETAILS

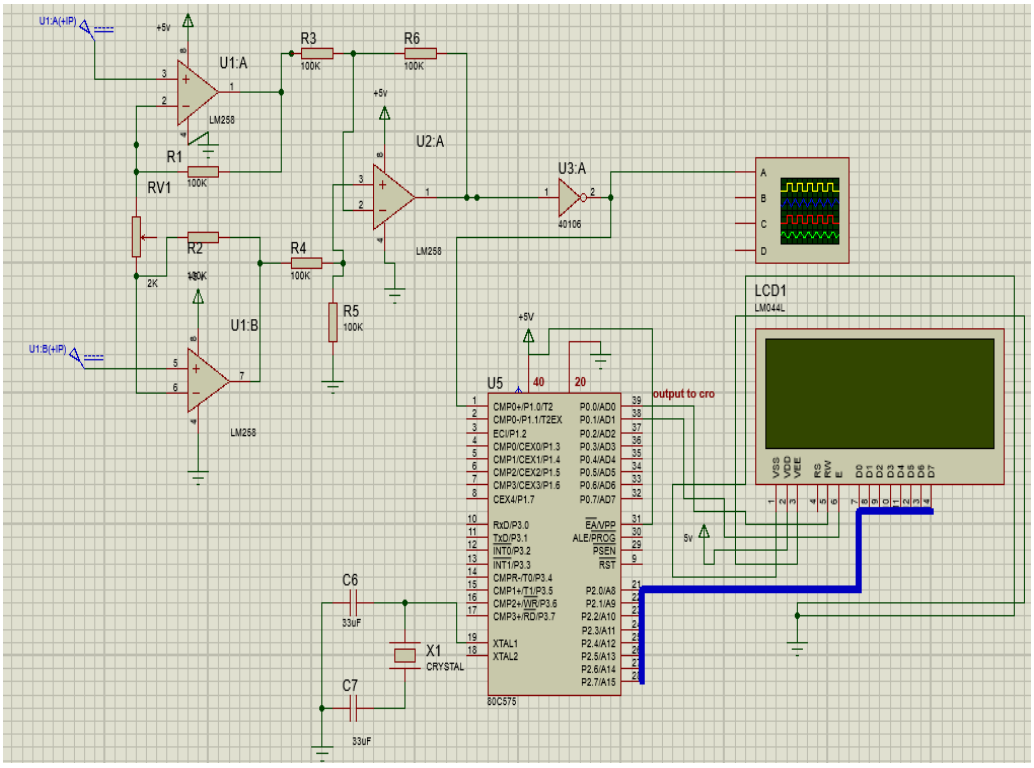

Figure 5. schematic of the digital system captured using the proteus software

The requirement is to develop the signal conditioning unit and capture the schematic of the whole system. The schematic of the digital speedometer is shown in figure F.

The whole unit consists of following elements:

- GMR sensor
- Signal processing hardware to convert the sensor signal output of 10mv to square pulses of +5V.
- Operational amplifier
- Schimtt trigger
- An 8 bit microcontroller with 40 pins. Display unit.

VII. DESIGN AND IMPLEMENTATION

The Figure 7 shows approach for implementing the FPGA design for the digital components. First Studying of the digital speedometer system and the identifying the components to be miniaturized that is functionality of the microcontroller. Then there are two methods to design the selected components. First method is based on frequency to speed conversion algorithm and second method is based on the constant elapsed constant time algorithm. Compare the result of the both two methods and then selecting the proper method to implement on the FPGA.

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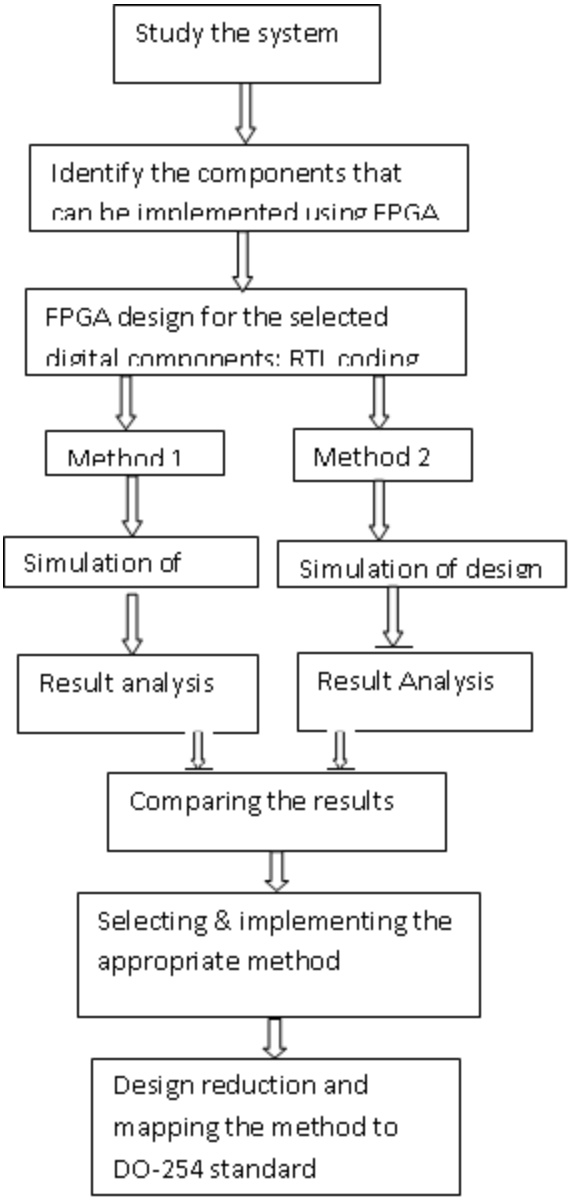

Figure 7. Project Flow

A. Method 1

First we considered the one pulse generation for one rotation i.e N=1. At the positive edge of input signal, the counter starts incrementing with respect to clock rate. Counter increments until next positive edge of input signal and stores the value into register. Time_count is a total time period of the input signal and it is calculated by multiplying the count value with clock period. Finally rotation per minute is calculated by dividing 60 with Time_count value.

B. Method 2

Second method for calculation of speed is based on the constant elapsed time (CET) method. CET algorithm is shown in figure 4.3. First we considered the sixteen pulse generation for one rotation of the motor i.e N=16. At the positive edge of input signal and at the positive edge of clock, counter starts incrementing till next positive edge of clock that is first we have to set the clock period of one second and stores the value of time_count in register. Finally a rotation per minute is calculated by dividing the time_count with sixteen and multiplies by 60.

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VIII. SIMULATION RESULTS

Simulation is the process of verifying the functional characteristics of models at any level of abstraction. To simulate the Hardware models and to test if the RTL code meets the functional requirements of the specification, if all the RTL blocks are functionally correct. This is achieved by using auto generated test bench, which generates clk, reset and required test vectors.

A. Simulation of Method 1

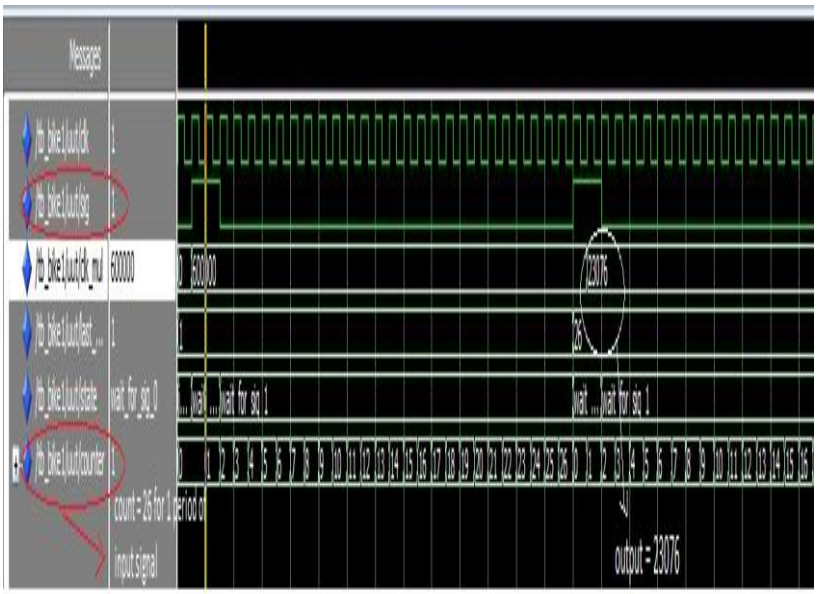

Figure 8. simulation results of method 1

Analysis of simulation result of method 1

- Simulation result for method 1 is shown in figure 8.
- First we considered the number of pulses is equal to 1 for 1 rotation of the motor and clock period is set as 1us.
- For every positive edge of the input pulse, the counter starts incrementing with reference to clock speed and it resets after reaching the next positive pulse.
- At point of next positive edge of input pulse, time period should be calculated by multiplying the counter value with clock period. and store it in another variable clk_mul.

Discussion: To get exact frequency, the variable clk_mul should be inversed. But division operation is not synthesizable in all FPGA's so we go for the method 2.

B. Simulation of Method 2

Analysis of simulation result of method 2

- Simulation result for constant elapsed algorithm that is method 2 is shown in figure 9.
- Input pulse is randomly generated and clock period is set to one second.
- We considered there are 16 pulses for one rotation of the motor.
- For the first period of clock, counter count1 increments with positive edge of input signal.
- For next clock period, counter count2 increments.

- These two counter values are added. Another counter cnt is used to set its value high for first clock period and low for next clock period.
- The output data_out contains the calculated value of the RPM. If there are 4 input pulses (data_in) then output data_out contains value 15.

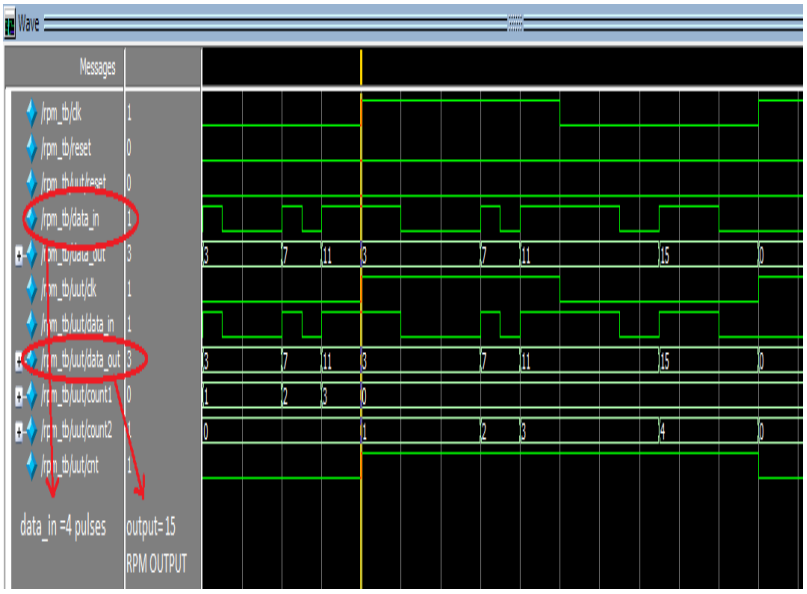

Figure 9. Simulation result of the method 2

IX. SYNTHESIS RESULTS

A. RTL Schematic

Below figure shows the top module of speedometer for method 1 calculation. The top module of CET algorithm (method 1) shows the number of inputs and outputs of the processor. DataIn is input and Dataout is output of 32 bit wide.

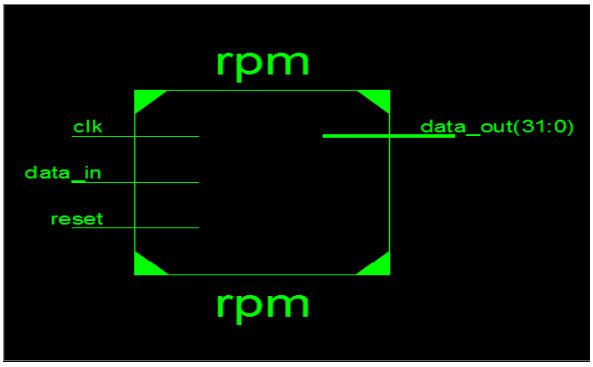

Figure 10. RTL Schematic of speedometer based on CET method at level 1.

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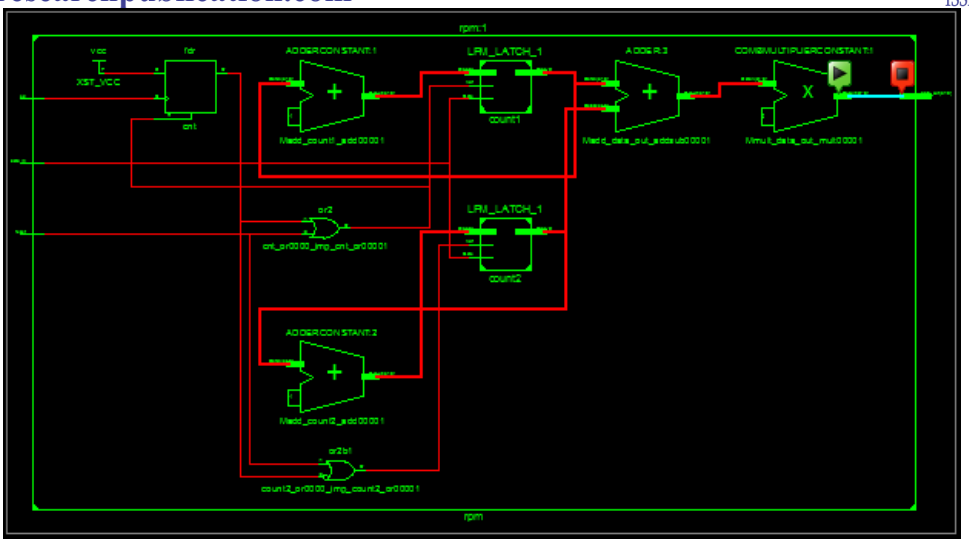

Figure 11. RTL Schematic of speedometer based on CET method at level 2

RTL View is a Register Transfer Level graphical representation of design. This representation is generated by the synthesis tool at earlier stages of a synthesis process when technology mapping is not yet completed. The goal of this view is to be as close as possible to the original HDL code. In the RTL view, the design is represented in terms of macro blocks, such as adders, multipliers and registers. Standard combinatorial logic is mapped onto logic gates, such as AND, NAND, and OR.

B. HDL Synthesis report

Synthesizing Unit <rpm_veri>.

Related source file is "rpm_veri.v".

Found 32-bit adder for signal <count1$add0000> created at line 56.

Found 32-bit adder for signal <count2$add0000> created at line 70.

Found 32-bit adder for signal <data_out$addsub0000> created at line 80.

Found 32x6-bit multiplier for signal <data_out$mult0000> created at line 80.

Summary:

inferred 1 D-type flip-flop(s).

inferred 3 Adder/Subtractor(s).

inferred 1 Multiplier(s).

Unit <rpm_veri> synthesized.

HDL Synthesis Report

Macro Statistics

# Multipliers	: 1
32x6-bit multiplier	: 1
# Adders/Subtractors	: 3
32-bit adder	: 3
# Registers	: 1
1-bit register	: 1
# Latches	: 2
32-bit latch	: 2

* Advanced HDL Synthesis *

Advanced HDL Synthesis Report

Macro Statistics

Multipliers : 1
32x6-bit multiplier : 1
Adders/Subtractors : 3
32-bit adder : 3
Registers : 1
Flip-Flops : 1
Latches : 2
32-bit latch : 2

Device utilization summary:

Selected Device : 3s400tq144-4

Number of Slices:	61	out of	3584	1%
Number of Slice Flip Flops:	65	out of	7168	0%
Number of 4 input LUTs:	116	out of	7168	1%
Number of IOs:	35			
Number of bonded IOBs:	35	out of	97	36%
Number of MULT18X18s:	2	out of	16	12%
Number of GCLKs:	2	out of	8	25%

X. CONCLUSION

Here, new approach is proposed for Digital speedometer using GMR sensor and addition to that improvement in miniaturization is achieved without affecting the functionality.

If the system is miniaturized then it has to be qualified according to DO-254 standards to be used in military or avionics. Performing verification to satisfy DO-254 at the board-level is not only challenging and risky, it is sometimes just not feasible within project timescales, we are mainly adopting a so-called in-hardware verification methodology. It is based on the use of a bit-accurate, in-hardware verification environment that can verify and trace the same FPGA-level requirements from RTL right through to the target device.

The improvement in the miniaturization without affecting the performance of earlier system can achieve by using other modern CMOS technology. The proposed improved embedded system in this thesis can be used in various applications like aerospace, automobile etc.

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