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A ROBUST DC-LINK VOLTAGE CONTROL STRATEGY TO ENHANCE THE PERFORMANCE OF SHUNT ACTIVE POWER FILTERS WITHOUT HARMONIC DETECTION SCHEMES

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ABSTRACT

Shunt active power filters (SAPFs) implementedwithout harmonic detection schemes are susceptible to sudden load variations. This paper proposes a robust control strategy to reduce this drawback. In this strategy, the dc-link voltage is regulated by a hybrid control technique combining a standard proportionalintegral PI and a sliding-mode (SM) controller. The SM schemecontinuously determines the gains of the PI controllerbased on the control loop error and its derivative. Thechattering due to the SM scheme is reduced by a transition rule that fixes the controller gains when steady state condition is reached. This controller is termed as dual-sliding-mode-proportional–integral. The phase currents of the power grid are indirectly regulated by doublesequencecontrollers with two degrees of freedom, wherethe internal model principle is employed to avoid referenceframe transformation. The proposed control strategyensures zero steady-state error and improves the performanceunder hard transients such as load variation. Additionally, it presents robustness when the SAPF isoperating under unbalanced conditions. Experimental resultsdemonstrate the performance of the proposed controlscheme.

Index Term: Adaptive control strategy, harmonic compensation, power factor correction, shunt active power filter (SAPF).

THE growing use of power converters as embedded devices in household, commercial, or industrial electronic-based appliances has deteriorated the power quality of the mains. Those nonlinear loads generate current harmonics and reactive power that result in voltage drops on the supply network impedance and may induce unbalance operating conditions. These effects can be even worse if the loads change randomly. Conventional solutions such as passive filters for reducing harmonic pollution are ineffective. Furthermore, the standards and recommendations that delimit the boundaries of harmonic distortion and reactive power in the power system have become more restricted [1], [2], which has stimulated the use of active power compensation [3], [4]. *SAPFs* have been extensively used for compensation of harmonics, reactive power, negative sequences, and/or flickers [5]–[7]. The conventional control schemes applied to *SAPF* are *HEBSs* because their effectiveness depends on how quickly and accurately the harmonic components of the nonlinear loads are identified [8].

Harmonic extractors used in *HEBSs* can be implemented by using different approaches such as traditional$d-q$ method [9] and $p-q$ theory [10], adaptive filters [11],wavelet [12], *GA* [13], or *ANN* [14]. The *SAPF* can be alsoimplemented without the use of the load harmonic extractors.In this case, the harmonic compensating term is obtained fromthe system active power balance [15]–[19]. These systems canbe considered as *BEBSs*, and their performance depends onhow fast the system reaches the equilibrium state [17].The control systems of *SAPF* implemented based on*HEBS* or *BEBS* concepts are generally accomplished bya cascade strategy composed by an inner control loop forregulating the filter phase currents (*HEBS*) or grid phasecurrents (*BEBS*) and an outer control loop to set the dc-linkvoltage. The effectiveness of both solutions depends on theperformance of the control loops. In the case of*HEBS*, the dclinkcontroller regulates the *dc* capacitor voltage at the suitablelevel to achieve the compensation objectives. Moreover, thecurrent control loop should regulate the *SAPF* phase currents,composed mainly of harmonic components, which requiresmore complex strategies for achieving suitable performanceindices. As for the case when *BEBS* is used, the dc-linkcontroller regulates the *dc* capacitor voltage and ensures thesystem active power balance, which in turn determines thereference currents of the power grid. As the power systemphase currents in steady state are basically composed of thefundamental component, the current control strategy used canbe simplified. Generally, *PI* controllers have been used forregulating the voltage of dc-link capacitors of both approaches.However, some alternatives to enhance *SAPF* dc-link performancehave been proposed, such as the feedforward schemesfor compensating the power grid voltage fluctuations [20] orthe use of adaptive control techniques for flexibility of reactivecompensation in hybrid active power filters [21]. Regardingthe current control loop, the technique to be used dependson the methodology employed. In the case of *HEBS*, thestandard solution employs *PI* controllers implemented in thecoordinates of the grid voltage vector reference frame [22].However, the use of these controllers results in steady-stateerrors, and the limitation of bandwidth has not allowed fora satisfactory harmonic compensation [23]. There are otherpossible solutions such as dead-beat control [24], SM control(*SMC*) [25], adaptive control [26], resonant control [27], andrepetitive-based control [28]. Among them, the latter seems tobe the most suitable in addition to having the advantage ofselective harmonic compensation. However, its implementationrequires a controller for the fundamental frequency and othersfor the remaining harmonic components, which can be quite expensive [29]. When the *SAPFs* are implemented according to the *BEBS* methodology, the current control strategy can be simplified by using only one resonant controller per phase, tuned at the fundamental frequency [17]. Recently, a different approach of an adaptive control strategy applied for *SAPF* using the *BEBS* methodology has been proposed for compensating the harmonic distortion, reactive power, and unbalanced load [17]. In this *SAPF*, the current control scheme is implemented by an adaptive pole placement control, integrated with a variable structure scheme ($V\ S\ -APPC$). The main advantage of the proposed control strategy refers to the reduction of *SAPF* complexity of implementation, resulting in reduced costs (because it is not necessary to have load and filter phase current measurements, thus reducing the number of current sensors), without reduction of its compensation effectiveness. However, this control scheme has a drawback that is the poor performance of the dc-link control loop during the occurrence of severe load variations. This paper proposes a robust control strategy to improve *BEBS* power filters during severe load changes. In this approach, the dc-link voltage is regulated by a hybrid control strategy composed by the association of a standard *PI* and an *SM* controllers. The *SM* scheme continuously determines the gains of the *PI*

controller based on the control loop error and its derivative. The chattering due to the *SM* scheme is reduced by a transition rule that fixes the controller gains when system steady state is reached. This new controller is termed as *DSM −PI*. The grid phase currents are indirectly regulated by *DSCs* with two degrees of freedom, where the *IMP*is employed to avoid reference frame transformation. These control structures ensure zero steady-state error in addition to presenting robustness to possible imbalances in the *SAPF* system. The proposed control strategy is very suitable for sampled data control and can be easily implemented on DSPs. The performance of the proposed control scheme is demonstrated with several experimental test results.

I. SYSTEM DESCRIPTION AND MODELING

Fig. 1 presents the topology of SAPF used in the laboratory prototype. It comprises a three-phase grid source es123 with its internal impedance (Zs= rs+ sls) that feeds a three-phase load bank consisting of parallel association of a noncontrolled rectifier and a three-phase linear load (Zl= rl+ sll). The SAPF is implemented with a V SI connected to the PCCthrough inductors lf (i.e., Zf= rf+ slf, wherein rfis the intrinsic resistance oflf).The control system program is executed in a DSP linked in with a PB that handles the measurement of the variables, as well as the converter drivers via OFLs.

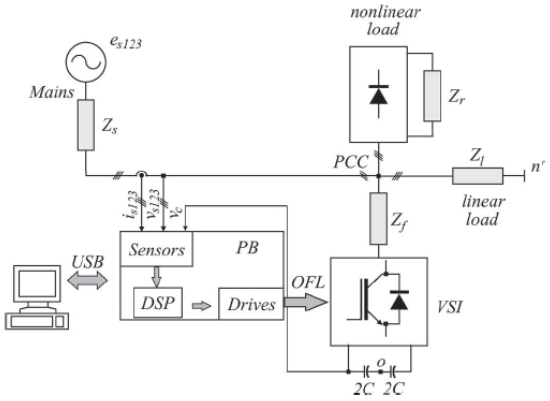

Fig. 1. Basic diagram of the proposed SAPF system.

A. SAPF Grid-Tied Power Converter Modeling

The model of the *SAPF* grid-tied power converter considering the interaction of the grid impedances to both the system Fig. 3.Equivalent circuit of the electrolytic capacitor. (a) Manufacturermodel. (b) Simplified model.
load and the filter was extensively studied in [17]. Based on this study, the system in Fig. 1 can be described by the perphase equivalent circuit presented in Fig. 2. In this circuit, the nonlinear load is represented by a current source *Ir*that represents the distorting currents generated by the rectifier. From the equivalent circuit shown in Fig. 2, the transfer function representing the dynamic behavior of power grid currents can be given by

$$G_c(s) = \frac{I^{s\prime}_{sdq}(s)}{V^{s}_{fdq}(s)} \approx -\frac{b_s}{s + a_s} \qquad (1)$$

where*bs*= 1/(*lf* + *ls*), and *as* = (*rf*+ *rs*)/(*lf* + *ls*). In this model, parameters *as* and *bs*may vary as a function of either the random behavior of nonlinear load or the grid impedances. Further details on the system modeling could be found in [17]. The *SAPF* in Fig. 1 employs aluminum electrolytic capacitors in its dc link to ensure a

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constant *dc* voltage *vC*. These capacitors are submitted to high-current ripple that can lead to self-heating and consequently modify its dynamic characteristics [30]. The overall dynamic performance of the *BEBS*-based solution is entirely dependent on the ability to keep a constant *dc* voltage at the dc link. Therefore, for the effective control of the *dc* bus voltage, it is necessary to describe the dynamic model of these capacitors. Such model can be represented by different electric models [30], [31]. The model chosen in this paper is shown in Fig. 3(a). It is the same used by manufacturers and also it is described by parameters easily identifiable.

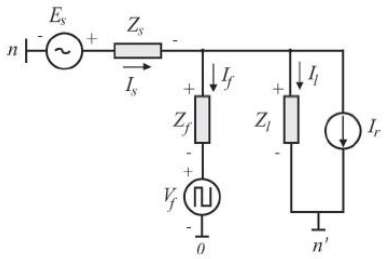

Fig. 2. Equivalent circuit of a SAPF system.

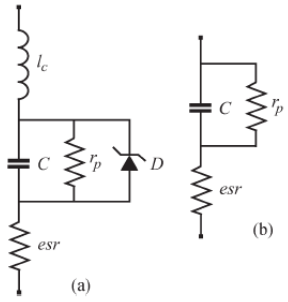

Fig. 3. Equivalent circuit of the electrolytic capacitor. (a) Manufacturer model. (b) Simplified model.

In this circuit, capacitance *C* decreases by increasing frequency. Resistance*esr*decreases by increasing frequency and temperature. Inductance *lc*is relatively independent of both frequency and temperature; it increases with terminal spacing. Resistance *rp*accounts for leakage current in the capacitor; it decreases by increasing capacitance, temperature, and voltage. The Zener diode *D* models the overvoltage and the reverse voltage behavior. Inductance *lc*has significant values when the switching frequency employed on the power converter is higher than 100 kHz. In applications with *SAPF*, the switching frequency used is far lower, and therefore, the inductance *lc*can be neglected from the model. The Zener diode *D* is also neglected because it does not affect the linear behavior of the capacitor. Thus, the equivalent circuit of the capacitor can be reduced to the one shown in Fig. 3(b). Based on this equivalent circuit, the dynamic model of the electrolytic capacitor can be given by

$$\frac{V_C(s)}{I_{sd}^e(s)} = \frac{esr\left(s + \frac{1}{r_pC} + \frac{1}{esrC}\right)}{s + \frac{1}{r_pC}}. \qquad (2)$$

The transfer function represented by (2) has a pole that depends on the values of *C* and *rp*and a zero depending on the values of *C*, *rp*, and *esr*. Considering a reasonable case where *rp*_ *esr*, it is possible to simplify the model given by (2), neglecting the value of *esr*. In this case, the resulting transfer function is given by

$$G_v(s) = \frac{V_C(s)}{I_{sd}^e(s)} = \frac{\frac{1}{C}}{s + \frac{1}{r_pC}} = \frac{b_c}{s + a_c} \qquad (3)$$

where*bc*= 1/*C*, and *ac* = 1/(*rpC*).

The dynamic behavior of both models varies depending on*C*, *rp*, and *esr*, which in turn vary as a function of frequency, voltage, and temperature.

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II. CONTROL SCHEME

Fig. 4 presents the block diagram of the proposed control scheme for the *SAPF* based on the methodology. In this block diagram, the dc-link voltage is regulated by a *DSM –PI* controller. It is done by generating the reference current $ie*sd$, which determines the system active power component. The phase angle of the power grid voltage vector $\theta s$is determined by using a *PLL*. Thus, the *dq*reference phase currents in a stationary reference frame *dqs*can be obtained by $is*sd=ie*sd\cos(\theta s)$ and $is*sq= ie*sd\sin(\theta s)$, respectively. The reference current $ie*sd$is defined to guarantee the active power balance of the *SAPF* system. The phase currents of the power grid are indirectly regulated by two *DSCs*, in which the *IMP* is employed to avoid reference frame transformations. The *DSCs* generate proper active filter phase voltages $vs*fd$and $vs*fq$. These *DSC* current controllers will be described next. The unmodeled disturbances *Isedq*and *Is_rdq*can be estimated and introduced into the algorithm of *DSC* current controllers. However, theoretical studies and experimental essays have shown that this control scheme has the ability of compensating such unmodeled disturbances. Block *xsdq*/123 performs the orthogonal transformation from the *dqs*reference frame to the three-phase system, i.e., from $vs*fdq$to $v*f123$. Based on thesereference voltages, a suitable *PWM* strategy determines theduty cycle of *V SI* power switches.

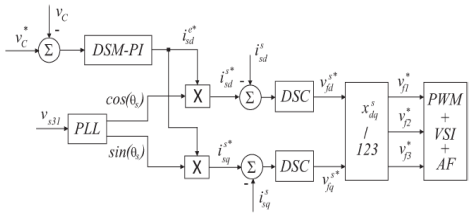

Fig. 4. Block diagram of the proposed control strategy. x^s_{dq} denotes voltage vector reference frame variables, whereas x^s_{dq} denotes stationary reference frame variables.

A. Grid Currents Control Strategy

The control strategy employed in this paper for regulating the grid currents (see block *DSC* in Fig. 4) is based on the doublesequence control scheme, which employs one controller for the positive sequence and another for the negative sequence [32].

Moreover, this controller has the advantage of using the *IMP* in its modeling that avoids the reference frame transformationwhile guarantees null steady-state error. Generically, the statespacemodel of the *DSC* can be represented by

$$\frac{dx^s_{1dqi}}{dt} = 2k_{ii}\varepsilon^s_{idq} + x^s_{2dqi} \qquad (4)$$

$$\frac{dx^s_{2dqi}}{dt} = -\omega_s^2 x^s_{1dqi} \qquad (5)$$

$$v^{s*}_{fdq} = x^s_{1dqi} + 2k_{pi}\varepsilon^s_{idq} \qquad (6)$$

where*kpi*and *kii*are the controller gains, and $\omega s$is the fundamental frequency of the power grid.

The transfer function of the current controller on the stationaryreference frame can be given by

$$C_c(s) = \frac{2k_{pi}s^2 + 2k_{ii}s + 2k_{pi}\omega_s^2}{s^2 + \omega_s^2}. \qquad (7)$$

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The design of the *DSC* is achieved by using the zeropole cancelation method. Therefore, considering that *as* can be associated to the current controller gains *kpi*and *kii*as

$$a_s \approx \frac{k_{ii}}{k_{pi}} \qquad (8)$$

the desired bandpass frequency of the *DSC* can be determined as *ωc= bskpi*. Thus, it is possible to determine the controller gains as a function of *as* and *bs*, which results in

$$k_{pi} = \frac{\omega_c}{b_s} \qquad (9)$$

$$k_{ii} = \frac{a_s \omega_c}{b_s}. \qquad (10)$$

Different design methodologies can be employed for calculating the current controller gains. Here, the proposed design approach achieves a good performance in the current control loop.

B. DC-Link Voltage Controller

The proposed control scheme for the dc link is implemented by a nonstandard robust *SM −PI*, which is implemented by a proportional–integral (*PI*) controller in which its controller gains are calculated by using the SMC approach based on the sliding surface composed by the control loop error and its derivative. The chattering due to the *SMC* scheme is reduced by a transition scheme, which fixes the controller gains when system steady state is reached. The inclusion of this transition scheme in the *SM −PI* controller results in a new controller that is termed here as *DSM −PI*.

1) SM −PI Control Scheme: Consider the dynamic

model of the dc link of the *SAPF* described by (3) with the value of *esr*neglected. Admitting that the *SM −PI* controller transfer function can be written as

$$C_v(s) = \frac{\widetilde{k}_p s + \widetilde{k}_i}{s} \qquad (11)$$

controller gains_ *kp*and_ *ki*are determined by *SMC* theory. Theclosed-loop dynamics of the dc-link voltage can be describedas follows:

$$V_c(s) = \frac{b_c k_p (s + k_i/k_p)}{s^2 + (a_c + b_c \widetilde{k}_p)s + b_c \widetilde{k}_i} V_c^*(s). \qquad (12)$$

During the transient state, the gain _ *kp*switches between*kavp* + 2*k*+*p* and *kavp*−2*k*+*p* . Upon reaching the steady state, _*kp* is kept constant at *kavp* . A similar statement applies to _ *ki*.Stability of the dc link is assured whenever

$$a_c + b_c \widetilde{k}_p > 0 \qquad (13)$$

$$b_c \widetilde{k}_i > 0. \qquad (14)$$

By using a suitable design procedure, these conditions can beeasily fulfilled.

Define a sliding surface described by

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$$\sigma = ce_v + \dot{e}_v \qquad (15)$$

where*ev*= *v*∗ *c*−*vc*, *e*˙*v*is its derivative, and *c* is a positiveconstant.

To prove the stability of the proposed *SM* −*PI* at the origin (σ = 0), let the Lyapunov candidate be

$$V(e_v) = \frac{1}{2}e_v^2. \qquad (16)$$

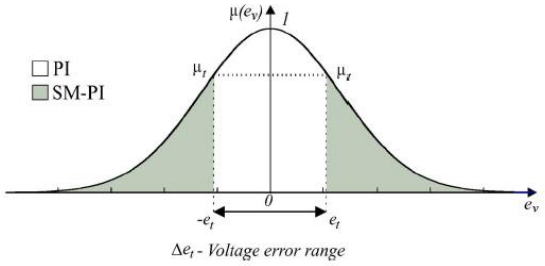

Fig. 5. Graph of the transition criterion μ.

Therefore, its time derivative can be expressed as

$$\dot{V}(e_v) = e_v\dot{e}_v = e_v(-ce_v) = -ce_v^2 < 0. \qquad (17)$$

Since constant *c* is positive, the proposed control is asymptoticallystable. Based on these stability restrictions, the controller gains can be determined by using the following switching laws:

$$\widetilde{k}_p = \left[(1+\text{sgn}(\sigma))\,k_p^+ - (1-\text{sgn}(\sigma))\,k_p^-\right] + k_p^{av} \qquad (18)$$

$$\widetilde{k}_i = \left[(1+\text{sgn}(\sigma))\,k_i^+ - (1-\text{sgn}(\sigma))\,k_i^-\right] + k_i^{av} \qquad (19)$$

where *k*+*p* , *k*−*p* , *k*+ *i* , *k*−*i* , *kavp* , and *kavi* are positive constants determined as a function of the desired system performance(these gains can be obtained by using a standard *PI* designmethodology, e.g., root locus). The mathematical functionsgn(σ) returns the values 1 for σ >0 or −1 for σ <0.

2) DSM −PI Control Scheme: The *SM −PI* controller has a good performance during the transient state but has an undesired side effect when the steady state is reached. It is the chattering originated by the *SMC* switching laws used for calculating the controller gains. This can be mitigated if the controller gains can be fixed in steady state (which results in a standard *PI* controller). It can be obtained by employing a transition rule in the controller structure. For this, consider a Gaussian function defined as

$$\mu(e_v) = e^{-\frac{e_v^2}{\lambda}} \qquad (20)$$

whereμ is the decision variable to select between the switchingand fixed controllers, *ev*is the dc-link voltage error, and λ is the parameter of the Gaussian function. Defining a range of values around the reference voltage of the dc link, i.e., Δ*et*, it is possible to calculate the value of μt= μ(*et*), from which the controller gains of *SM −PI* are fixed (i.e.,*kp*= *kavp* and _*ki*= *kavi*), as demonstrated in

Fig. 5. In this graph, the value μtrepresents the threshold related to voltage error *et*where the controller transition must occur. Therefore, the transition works as follows: By using (20), the value of μ(*ev*) is continuously calculated for each error voltage *ev*. If this value is smaller than μt, the implemented controller is the *SM −PI*;

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otherwise, it is employed a standard *PI* with antiwindup (controller *SM* −*PI* with fixed gains). To make this transition smooth, it is necessary to adequately adjust parameter λ. The higher λ, the less sensitive is μ to the voltage error *ev*; otherwise, the smaller λ, the more sensitive will be μ to the voltage error *ev*.

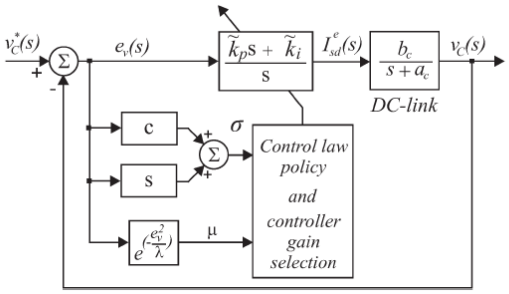

Fig. 6.Block diagram of the *DSM* − *PI* control scheme.The_*kp*and_*ki* gains updating policy is as follows: for $\mu(ev) < \mu t$, the gains change according to (23) and (24), and for $\mu(ev)$ _ μt, the gains are kept constant.

The block diagram of the proposed *DSM* −*PI* controlleris shown in Fig. 6. In which, the *DSM* −*PI* controller gains _*kp* and _

*ki*are determined by switching laws of (18) and (19)

obtained from the sliding surface determined by blocks *c* and *s*.

3) Design Criteria of the DSM −*PI:* The design criterion employed in this paper is based in the pole assignment that requires the solution of the Diophantine equation. Thus, consider the transfer functions of dc link [see (3)] and thevoltage regulator *DSM* −*PI* [see (11)] can be written in termsof polynomials

$$G_v(s) = \frac{Z(s)}{R(s)} \tag{21}$$

$$C_c(v) = \frac{P(s)}{L(s)} \tag{22}$$

where $Z(s) = b_c$, $R(s) = s + a_c$, $P(s) = \tilde{k}_p s + \tilde{k}_i$, and $L(s) = s$. Then, the transfer function of the dc-link control loop will be given by

$$T_{et}(s) = \frac{Z(s)P(s)}{Z(s)P(s) + R(s)L(s)} \tag{23}$$

whose characteristic equation is

$$Z(s)P(s) + R(s)L(s) = 0. \tag{24}$$

The design objective is to find suitable polynomials $P(s)$ and $L(s)$ such that

$$Z(s)P(s) + R(s)L(s) = A^{\eta*}(s) \tag{25}$$

where$A\eta*(s)$ is a desired harmonic Hurwitz polynomial, and superscript $\eta \in \{fs(\text{fast}), av(\text{average}), sl(\text{slow})\}$ refers to the performance criteria employed for determining desired polynomials. Once the suitable polynomials $A\eta*(s)$ are defined, the voltage regulator parameters can be obtained from the solution of the Diophantine equation. The design criterion first determines the slow polynomial ($Asl*(s)$) from the nominal parameters of the plant [see (3)], considering the performance indexes of maximum overshoot *Mp*= 5% and the damping coefficient of $\xi = 0.707$. Thus, the following polynomial can be obtained:

$$A^{sl*}(s) = s^2 + 2a_m^{sl} + 2\left(a_m^{sl}\right)^2 \tag{26}$$

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TABLE I
SYSTEM PARAMETERS

$E_s = 110V(rms)$	$f_s = 60Hz$
$r_s = 0.2$	$l_s = 0.1mH$
$r_f = 2\Omega$	$l_f = 1mH$
$r_l = 40\Omega$	$l_l = 30mH$
$C = 2200\mu F$	$f_{sw} = 10kHz$

where*aslm* = 4/*tslss*(2%), and *tslss*(2%) = *tnss*(2%) is the nominalsettling time of system steady state. To determine the amplitudesof the switching laws given by (18) and (19), two otherpolynomials (i.e., $Aav*(s)$ and $Afs*(s)$) are also defined, whichcorrespond to a reduction of 40% and 62.5% of the nominalsteady state time (*tslss*(2%)), respectively. Taking into accountthese three polynomials and solving the Diophantine equationsfor each case, the following gains can be obtained:

$$k_p^{\eta} = \frac{2a_m^{\eta} - a_c}{b_c} \tag{27}$$

$$k_i^{\eta} = \frac{2\left(a_m^{\eta}\right)^2}{b_c} \tag{28}$$

where k_p^{η} and k_i^{η}, with $\eta \in \{fs, av, sl\}$ referring to the controller gains obtained from the polynomials $A^{\eta*}(s)$. Therefore, it is possible to determine the coefficients k_p^+, k_p^-, k_i^+, and k_i^- as follows:

$$k_p^+ = \frac{k_p^{fs} - k_p^{av}}{2} \qquad k_i^+ = \frac{k_i^{fs} - k_i^{av}}{2} \tag{29}$$

$$k_p^- = \frac{k_p^{av} - k_p^{sl}}{2} \qquad k_i^- = \frac{k_i^{av} - k_i^{sl}}{2}. \tag{30}$$

III. EXPERIMENTAL EVALUATION OFTHE PROPOSED *SAPF*

The proposed control system presented in Fig. 4 has been experimentally evaluated by using a 10-kW three-phase active power filter laboratory prototype. It is composed by a threephasepower grid feeding a nonlinear load. The *V SI* is connected to the *PCC* by using input filter inductors *lf* = 1.0 mH. The dc link is composed by capacitors of 2200 μF with a rated voltage of 410 V. The nonlinear load is implemented by a three-phase rectifier, feeding an *RL* load (i.e., *rl*= 40 Ωand *ll*= 30 mH). The derivative of the load current reaches 16.32 kA/s, with total harmonic distortion (*THD*) = 21.5%and a lagging power factor of 0.89. The proposed control system was implemented on a *TMS*283335 *DSP* platform. The *A/D* converters of the *DSP* card are connected to a measurement unit, composed by Hall effect voltage and current sensors. The signal taken from these sensors passes through a first-order low-pass filter with cutoff frequency of *f*LPF=2.5 kHz for antialiasing purposes. The control algorithm is implemented in C++ and executed with a sampling time of 100 μs. The *SAPF* parameters of the laboratory prototype are provided in Table I.

Different conditions with hard transient and sudden loadvariations were considered in order to validate the theoretical studies developed in this manuscript. In additional comparison with a conventional *PI* controller was done to highlight thebenefits of the proposed technique. The following scenarios were investigated: *a*) start-up charging the dc-link capacitor; *b*) transient of the dc-link reference voltage with both step up and step-down variations; *c*) hard load transient variation by increasing and reducing the load power; *d*) unbalanced grid voltage; and finally *e*) reactive power compensation.The parameters of the *DSM* $-PI$ controller employed inthe experimental tests are presented in Table II.

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TABLE II
$DSM - PI$ CONTROLLER PARAMETERS

$k_p^+ = 0.033$	$k_p^- = 0.022$	$k_p^{av} = 0.11$
$k_i^+ = 2.145$	$k_i^- = 0.88$	$k_i^{av} = 2.75$
$c = 100$	$\lambda = 500$	$\mu_t = 0.98$

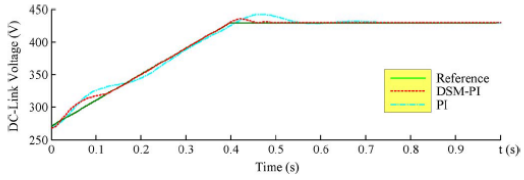

Fig. 7. Experimental result for dc-link voltage v_C during startup.

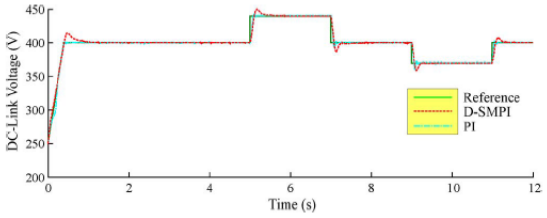

Fig. 8. Experimental result for dc-link voltage v_C during step transient of its reference voltage with both step-up and step-down variations.

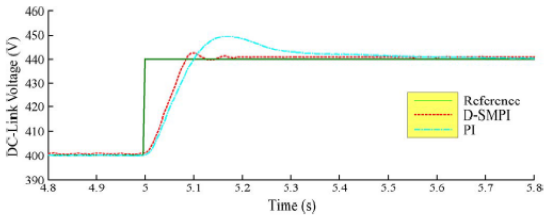

Fig. 9. Experimental result for dc-link voltage v_C during step transient of its reference voltage.

IV. CONCLUSION

This paper has proposed a control approach for improving the performance of *SAPF* without load current measurements.

In this control approach, the dc-link voltage is regulated by a dual control scheme implemented by proportional–integral (*PI*) controller with the gains calculated by using an SMC approach. The chattering due to the *SM* can be mitigated by using a transition rule in the controller structure. The theoretical bases of the *SM − PI* was introduced, and the stability proof was presented. Moreover, the transition scheme that results in *DSM − PI* was also discussed. With this control strategy, the performance of the dc-link control loop during the load variations is enhanced. The phase currents of the power grid are indirectly regulated by two independent controllers (*DSCs*), in

which the IMP is employed to avoid reference frame transformations. This demonstrates that there are significant gains in the *SAPF* based on the *BEBS* since the current control strategy is simpler and the filter control strategy is implemented with reduced number of current sensors. A comprehensive set of

experimental results demonstrates the effectiveness of the proposed control strategy even during system load variation while providing simultaneously system reactive power compensation and harmonic mitigation.

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