International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

DESIGN AND ANALYSIS OF VEDIC MULTIPLIER USING MICROWIND

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ABSTRACT

Multiplication is the fundamental operation in Arithmetic and logical unit. In this paper we have designed a multiplier unit which is important part of ALU. In basic multiplication required addition, subtraction and shift operation. Simple linear multipliers had been designed already. But for fast multiplication, there is technique used Vedic mathematics in which delay and area increases very slowly as the number of bits increases. In this paper multiplier circuits have designed in DSCH tool and simulated in Microwind using CMOS 180nm technology. Simple Braun Array and Vedic multipliers are compared in terms of power, delay and area. By the analysis of multiplier circuits using Microwind tool found that the delay of proposed Vedic multiplier is reduced by 69.8%.Hence it gives better performance that Braun Array multiplier.

Keywords: Area, Braun Array multiplier, CMOS technique, Delay, Full adders, Power dissipation.

I. INTRODUCTION

In VLSI designs today, the device dimensions are shrinking exponentially and the circuit complexity is also growing. Further, device scaling is limited by the power dissipation, demanding for better power optimization technique. As the scale of integration keep growing, more and more signal processing systems are being implemented on VLSI chips. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance, area becomes major design goals, power consumption has become important parameter in today's VLSI system design.

An ALU is a fundamental building block of a central processing unit in any computing system. The ALU perform the arithmetic operations such as addition, multiplication etc. So the need of fast multiplication is important in DSP systems. In basic multiplication required addition, subtraction and shift operation. But for fast multiplication, there is technique used Vedic mathematics technique in the number of bits increases. Low power multipliers (parallel and serial) have wide applications in signal processing. Therefore Braun array multiplier and Vedic multipliers has been designed and provide good area optimization and less power dissipation. CMOS technique is used for full adders and multipliers design. All the circuits are designed in DSCH and simulated in Microwind tool. Braun array and Proposed Vedic multipliers are compared in terms of power, delay and area.

II. ANALYSIS OF ADDERS

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. Adders are essential not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. There is a necessity of Fast adders in

ALUs, for computing memory addresses, and in floating point calculations. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. The most important for measuring the quality of adder designs in the past were propagation delay, and area.

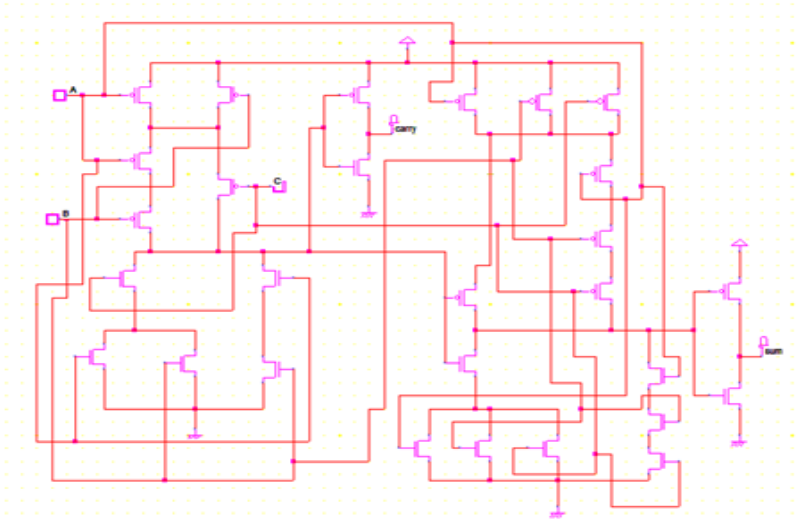

Figure 1.1 Full adder

III. ANALYSIS OF MULTIPLIERS

Braun Array Multiplier:- The simplest parallel multiplier is the Braun array. All the partial products are computed in parallel, and then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. Braun array multiplier consist of AND gates and full adders. Each of a_i x b_i product bits is arranged in parallel with AND gates. Each partial product can be added to previous sum of partial product.

Vedic mathematics multiplication technique

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on following algorithm, which is discussed below:

Technique used

Urdhva Tiryakbhyam Sutra

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products.

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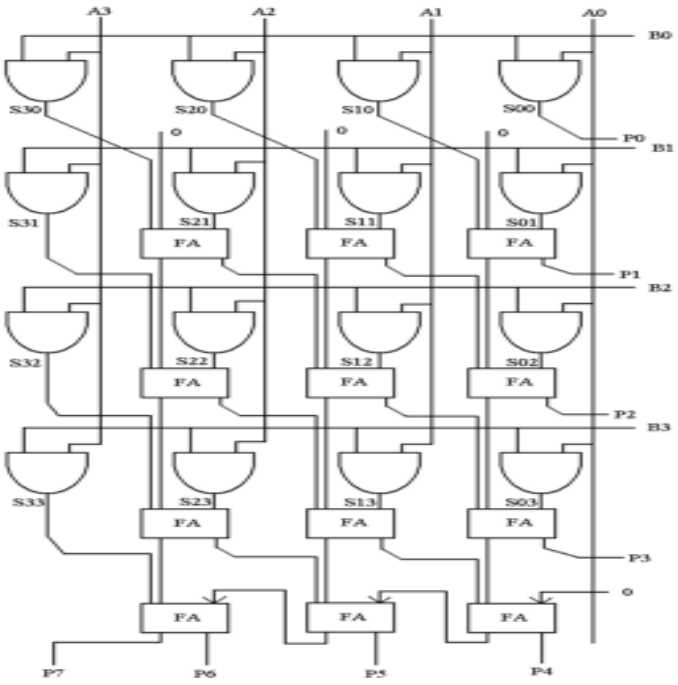

Figure 1.2 Braun array multiplier

1) Multiplication of two decimal numbers- Line diagram

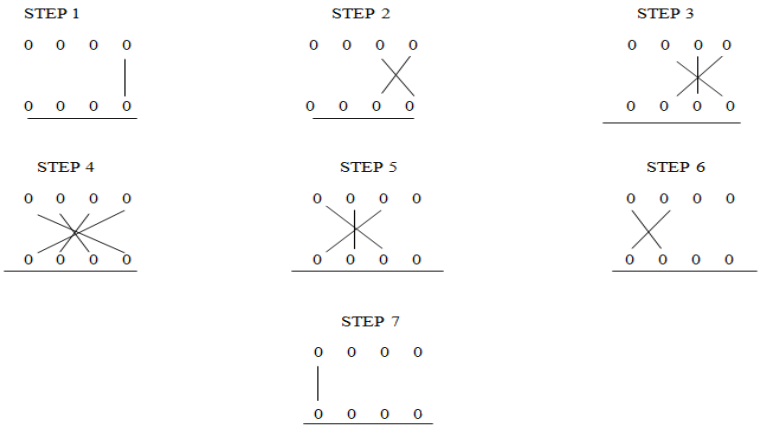

Figure 1.3 Line diagram for Vedic multiplication

IV. PERFORMANCE PARAMETERS

1) Power Dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its input. The D.C or average power dissipation is the product of D.C supply voltage and the mean current taken from the supply.

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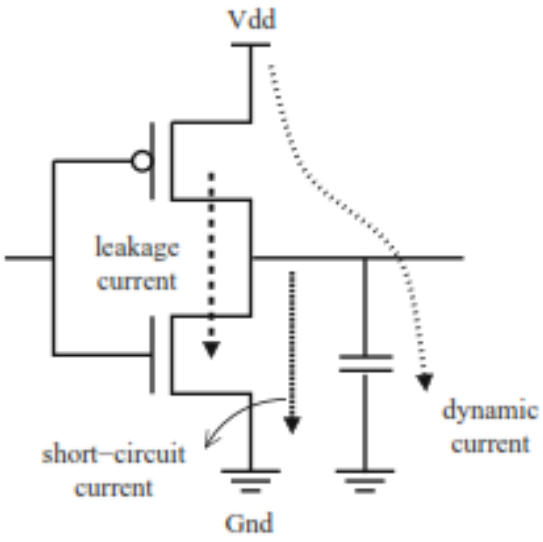

Figure 1.4 Power dissipation in cmos

2) Delay

The delay can be defined as time required to reach 0.5 Vdd of output from the 0.5V of input.

Delay of multiplier= $(n-1)*m*T_{full\ adder}$ n=number of multiplicand

3) Area

The area needed for Vedic square multiplier is very small as compared to other multiplier architectures i.e. the number of devices used in Vedic square multiplier are 259 while Booth and Array Multiplier is 592 and 495 respectively. Thus the result shows that the Vedic square multiplier is smallest and the fastest of the reviewed architectures

V. SIMULATION RESULTS

Braun array multiplier:

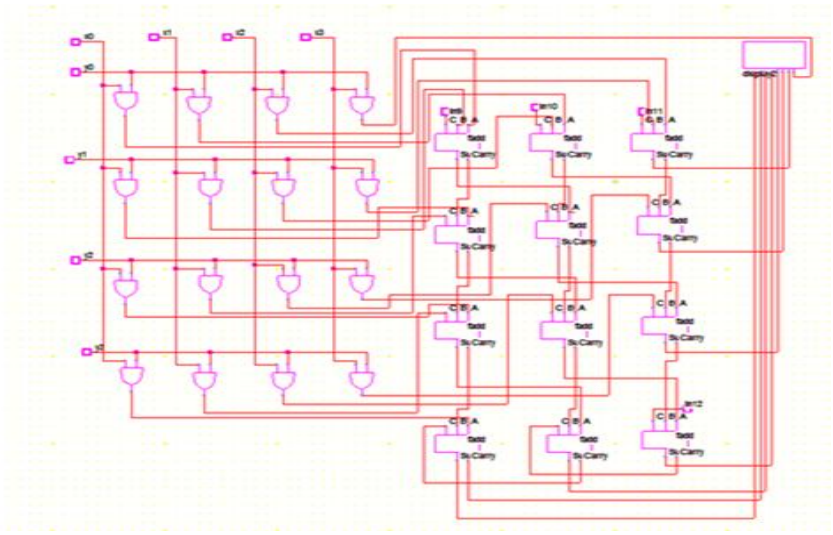

Figure 1.5 Schematic of Braun Array multiplier

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WAVEFORM:-

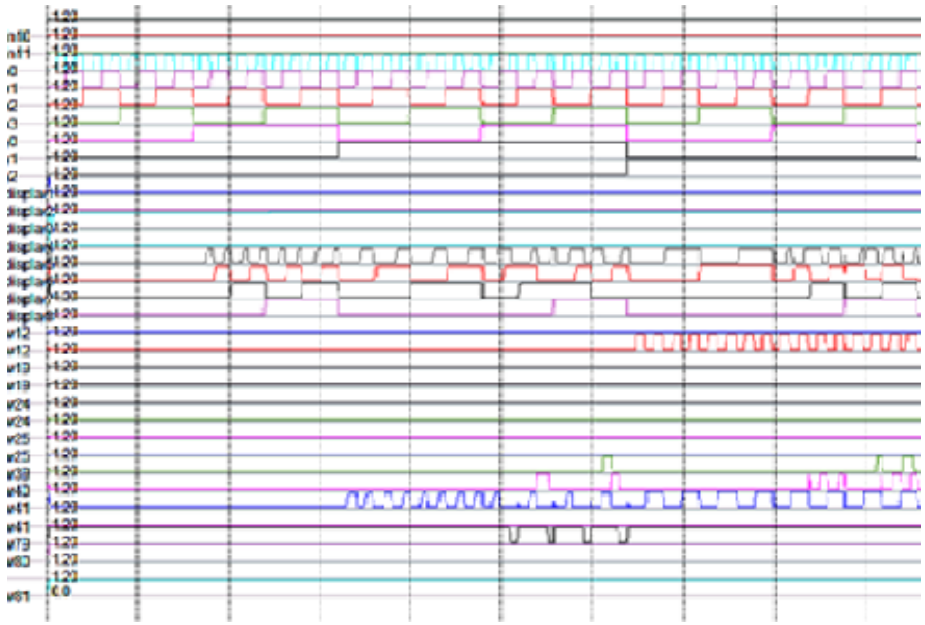

Figure 1.6 output waveform of Braun array

LAYOUT:-

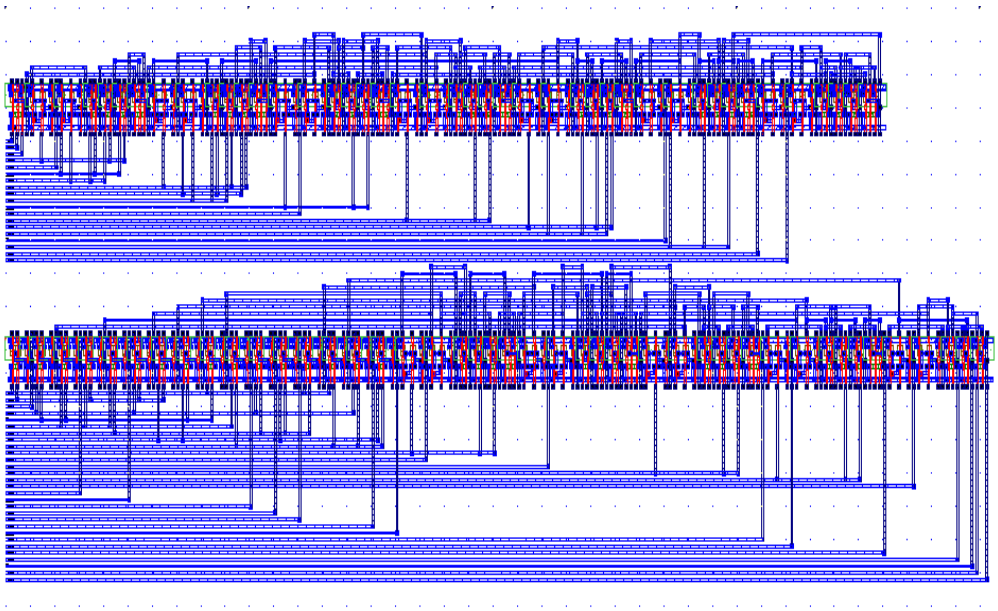

Figure 1.7 Layout of Braun array multiplier

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Proposed Vedic Multiplier

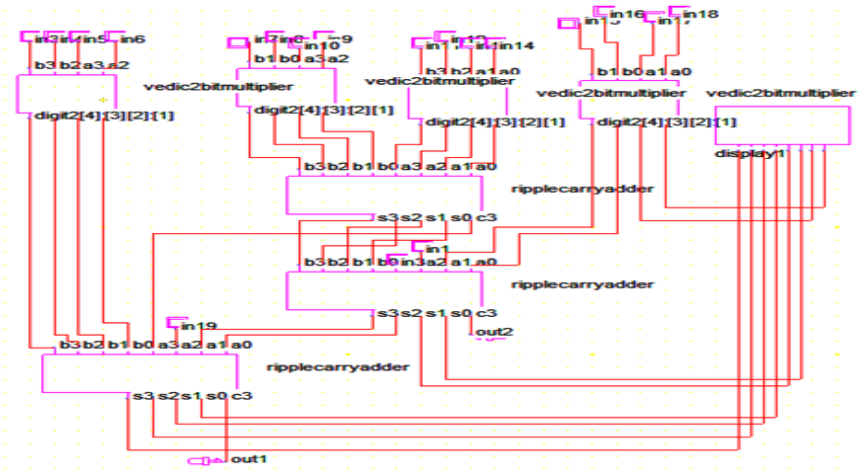

Figure 1.8 Schematic of 4 bit Vedic multiplier

WAVEFORM:-

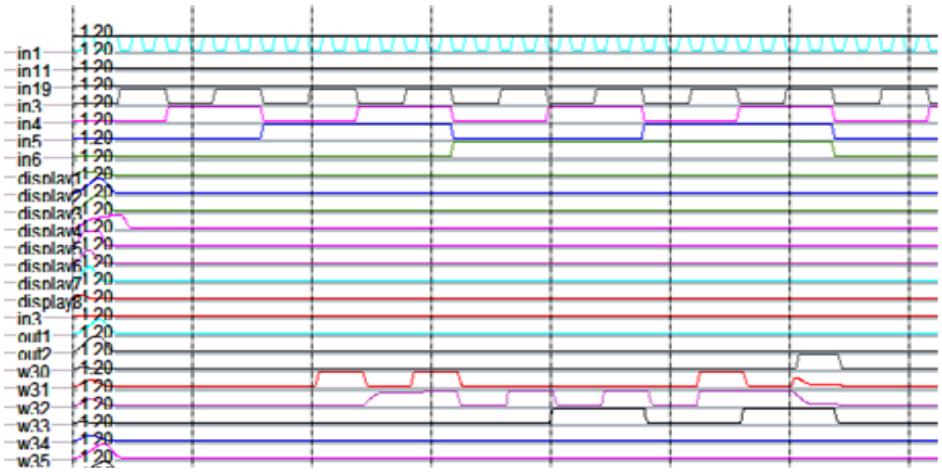

Figure 1.8 Output waveform of Vedic multiplier

LAYOUT:-

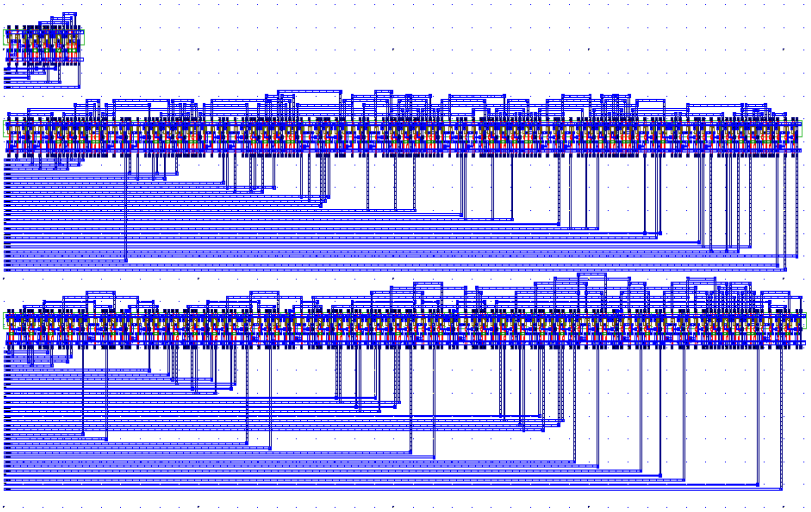

Figure 1.9 Layout of Vedic multiplier

VI. COMPARISON AND DISCUSSION

There are different types of multipliers are designed using 180nm.

4*4 multipliers 180nm technology (BSIM4 model)

Multipliers	Width (um)	Height (um)	No. Of PMOS	No. of NMOS	S.Area (um^2)	Power Diss.(mw)	Delay(ps)
Braun array	122	31	228	228	4522	0.509	38
Vedic multi.	124	32	248	248	5047	0.156	96

Table 1.1

Simulation results of Braun array multiplier and Vedic multiplier compared in the terms of power, delay and area. Width and height of layouts are changes according to technology.

VII. CONCLUSION

The proposed Vedic multiplier is designed using CMOS technique and it performed with 69.35 less power dissipation as compared to Braun array multiplier. The no of transistor count increases but gives less delay and high speed as compare to other multipliers. Vedic Multipliers are used in fields of Digital Signal Processing (DSP), Chip Designing, Discrete Fourier Transform (DFT), and High Speed Low Power VLSI circuits. In future power reduction is main aim for digital design.

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