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# DESIGN OF HIGH SPEED AND ENERGY EFFICIENT CARRY SKIP ADDER

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## ABSTRACT

*Adders are a key building block in Arithmetic and logic units and therefore increasing their speed and minimizing their power has a strong impact on speed and power consumption of processors. Among the conventional adders such as RCA, CIA, CSLA, PPA, the Carry skip adder (CSKA) is an efficient adder in terms of power consumption and area usage as the critical path delay and power-delay product of CSKA is small compared to other conventional adders. However the use of Multiplexer for Carry skip logic in CSKA causes increase in power consumption due to the use of large number of Transistors. Hence, an power efficient CSKA called Concatenation-Incrementation (CI-CSKA) has been proposed. In CI-CSKA, The power reduction can be enhanced by replacing the Multiplexer that is used to skip the carry with Or-And-Invert (OAI)/And-Or-Invert(AOI) logic. As the number of transistors is reduced to half by using AOI/OAI logic when compare to MUX, Power reduction is achieved without compromising the speed making it suitable for wide range of low-power applications. The CSKA and CI-CSKA adders are implemented in 45-nm static CMOS technology and simulated using Synopsys HSPICE simulations and their performances are compared in terms of power, delay and power-delay product.*

***Index Terms: Carry skip adder (CSKA), energy efficient, highper formance, hybrid variable latency adders, voltage scaling***.

## I. INTRODUCTION

The ever-increasing demand for mobile electronic devices requires use of power-efficient VLSI circuits. Computations in these devices need to be performed using low-power area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation and it plays a vital role in filter designs, processors and DSP applications.

In general, adders are commonly found in the critical path of microprocessor designs and Digital Signal Processing-chips. Adders are essential not only for addition, but also for subtraction, multiplication, and division. A fast and accurate operation of the digital system is greatly influenced by the performance of the resident adders. The most important for measuring the quality of adder designs in the fast were propagation delay, and area.

One of the most efficient architectures in terms of area and power dissipation is the carry-skip adder (CSKA). In fact, its speed is much higher than simple ripple carry adder (RCA), while being almost equivalent in terms of

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low area and power dissipation. Moreover, the CSA is characterized by a good efficiency in the tradeoff between power dissipation and speed, since it has a low power-delay product, close to that of a carry-look ahead adder (CLA).

The Carry Skip Adder (CSKA) is considered as the efficient Adder as its area usage and power consumption is same as RCA but the critical path delay is small compared to RCA. The speed limitation of CSKA limits it use in high-speed applications. Different strategies are applied to conventional CSKA to make it efficient in terms of speed and power consumption.

A CSKA consists of full adder gates grouped together into blocks, whose configuration (i.e., the number of full adders per block) strongly affects the overall speed. The blocks are connected by 2:1 multiplexers, which can be placed into one or more level structures.

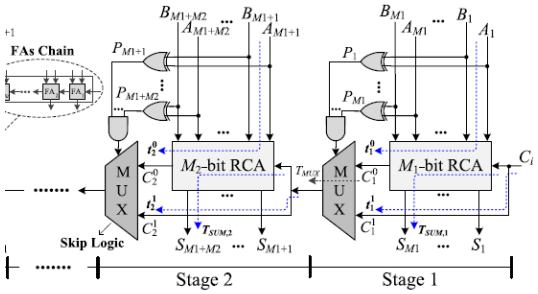


**Fig 1.Conventional carry skip adder**

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The Multiplexer is used to skip the logic to next stage. In addition to the chain of FAs in each stage, there is carry skip logic. For an RCA that contains N cascaded FAs, the worst propagation delay of the summation of two N-bit numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

Pi=Ai XOR Bi (1)

## II. CI-CARRY SKIP ADDER

The structure is based on combining the concatenation and the incrementation schemes. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one.

The adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size of Mj*(j*= 1. . . Q*)*. In this structure, the carry input of all the RCA blocks, except for the first block which is *C*i, is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously. In this structure, when the first block computes the summation of its corresponding input bits (i.e., SM1. S1*)*,and C1, the other blocks simultaneously compute the intermediate results [i.e., {ZK j+Mj, . . . , ZK j+2, ZK j+1} form j =_j−1 *r*=1 Mr *(* j = 2, . . . , Q*)*], and also Cj signals. In the proposed structure, the first stage has only one block, which is RCA. The stages 2 to Q consist of two blocks of RCA and incrementation. The incrementation block uses the intermediate results generated by the RCA block and the carry output of the previous stage to calculate

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the final summation of the stage

This problem, in the proposed structure, has used an RCA block with a carry input of zero (using the concatenation approach). This CO way, since the RCA block of the stage does not need to The skip logic determines the carry output of the j th stage (, j ) based on the intermediate results of the j th stage and the carry output of the previous stage (CO, j−1) as well as the carry output of the corresponding RCA block (Cj*)*. When determining CO, j, these cases may be encountered. When Cj is equal to one, CO, j will be one. On the other hand, when Cj is equal to zero, if the product of the intermediate results is one (zero), the value of CO, j will be the same as CO, j−1 (zero).

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. In the Conv-CSKA, the skip logic is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block. To solve wait for the carry output of the previous stage, the output carries of the blocks are calculated in parallel.

The chain of the FAs of the first stage, the path of the skip logics, and the incrementation block in the last stage. The delay of this path (TD*)* may be expressed as

TD= [M1 TCARRY] + [(Q-2) TSKIP] + [(MQ-1) TAND + TXOR] (2)

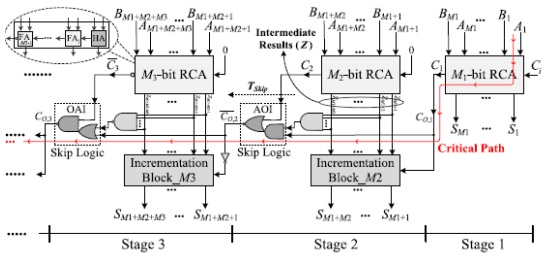


**Fig 2.CI-carry skip adder.**

## III. PROPOSED HYBRID VARIABLE LATENCY CSKA

The basic idea behind variable latency adders is that the critical paths of the adders are activated rarely. Hence, the supply voltage may be scaled down without decreasing the clock frequency. If the critical paths are not activated, one clock period is enough for completing the operation. In the cases, where the critical paths are activated, the structure allows two clock periods for finishing the operation. Hence, in this structure, the slack between the longest off-critical paths and the longest critical paths determines the maximum amount of the supply voltage scaling. Therefore, in the variable latency adders, for determining the critical paths activation, a predictor block, which works based on the inputs pattern, is required.

The concepts of the variable latency adders, adaptive clock stretching, and also supply voltage scaling in an *N*-bit RCA adder. The predictor block consists of some XOR and AND gates that determines the product of the propagate signals of considered bit positions. Since the block has some area and power overheads, only few middle bits are used to predict the activation of the critical paths at price of prediction accuracy decrease the input bits ( *j*+ 1)th–( *j* + *m*)th have been exploited to predict the propagation of the carry output of the *j* th stage (FA) to the carry output of ( *j* +*m*)th stage. For this configuration, the carry propagation path from the first stage to the *N*th stage is the longest critical path (which is denoted by Long Latency Path (LLP), while the carry

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propagation path from first stage to the ( *j*+*m*)th stage and the carry propagation path from ( *j* +1)th stage to the *N*th stage (which are denoted by Short Latency Path (SLP1) and SLP2, respectively) are the longest off-critical paths. It should be noted the paths thatthe predictor shows are (are not) active for a given set of inputs are considered as critical (off-critical) paths. Having the bits in the middle decreases the maximum of the off-critical paths. The range of voltage scaling is determined by the slack time, which is defined by the delay difference between LLP and max(SLP1, SLP2). Since the activation probability of the critical paths is low (<1/2*m)*, the clock stretching hasa negligible impact on the throughput (e.g., for a 32-bit adder, *m* = 6–10 may be considered). There are cases that the predictor mispredicts the critical path activation. By increasing *m*, the number of misprediction decreases at the price ofincreasing the longest off-critical path, and hence, limiting the range of the voltage scaling. Therefore, the predictor block size should be selected based on these tradeoffs.

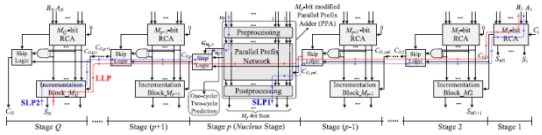

**Fig3.Hybrid variable latency CSKA**

## IV. SIMULATION RESULTS

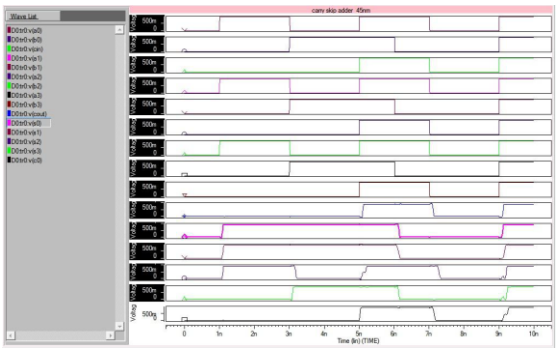

**Fig4.4-bit carry skip adder**

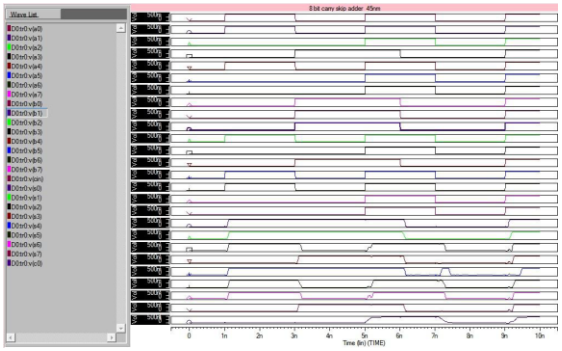

**Fig5.8-bit carry skip adder**

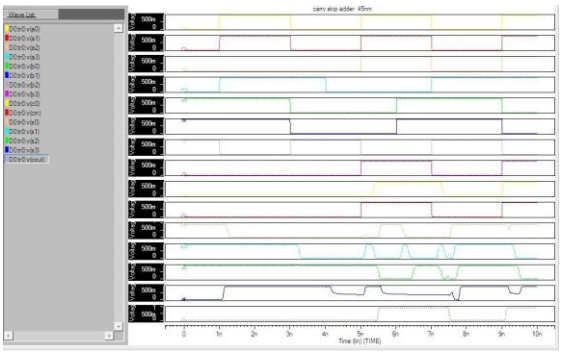

**Fig 6. 4-bit CI-carry skip adder.**

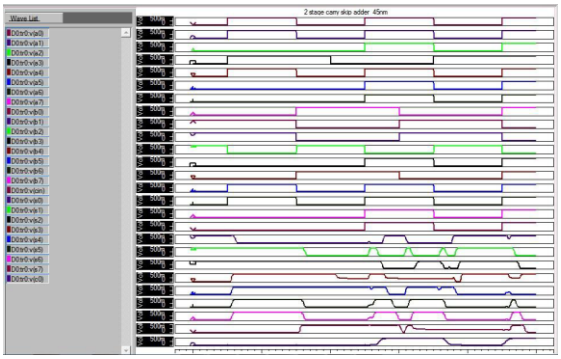

**Fig7.8-bit CI-carry skip adder.**

## V .CONCLUSION

A new adder named CI-CSKA has been designed which achieves high speed computation with less power consumption. The proposed CI-Carry Skip Adder achieves 20.2% reduction in power and 80.45% reduction in

delay compared to all conventional adders thereby making suitable for all high speed and low power.

To simulate the out performs and provides significant improvement Power, area, and delay.

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