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DESIGN AND IMPLEMENTATION OF LOW POWER LEVEL SHIFTER

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ABSTRACT

Multi supply voltage design technique is widely used in modern system on chips to trade-off energy and speed. Level shifters (LSs) allow different voltage domain to be interfaced. The proposed system is presented for fast and low power consuming level shifter. Since the system combines with multi threshold CMOS technique the proposed technique guarantees robust voltage shifting. This system exhibits fast response and low energy consumption. The level shifter is designed using 90nm CMOS technology. Synopsys HSPICE is to be used to simulate the circuit design. Performance metrics of this level shifter is delay, power and power delay product

Keyword: Differential Cascade Voltage Switch Logic(DCVL),(High Threshold Voltage (Hvt),Level Shifter (LS), Low Threshold Voltage (Lvt), Multi Supply Voltage Design (MSVD).

I. INTRODUCTION

Real time monitoring systems like hearing aids, pace-makers, cochlear implants, electrocardiogram, thermal monitors, environmental wireless sensors and some other devices require very less power in order to operate with long lifetime even from small constrained batteries. Power constraints of the above devices are most important. Power consumption in VLSI circuits includes dynamic, static and leakage power consumption. Dynamic power consumption is due to switching of load capacitance between two different voltages and it depends on frequency of operation. Static power consumption is due to direct short circuit between supply and ground .leakage power is due to substrate injection and at sub threshold. So more attention is to be paid towards leakage power reduction.

Power consumption of a system can be reduced much if the supply voltage is well below the device threshold voltage. This is said to be sub threshold operation. Multi supply voltage domain(MSVD) is an another technique to reduce both dynamic and leakage power.MSVD is the process of portioning the design into separate voltage domains, each will operate at a proper power supply voltage level depending on its timing requirements. Some part of the domain will operate in sub threshold domain and some other part of the circuit will operate in above threshold regime. Even the whole circuit operates at sub threshold regime secondary above threshold regime is needed to digital I/O pad cells. Also analog pad cells cannot be directly connected to the sub threshold regime. Level shifters are still be needed externally to connect sub threshold chips to logic analyzers. So a resource efficient on chip level shifters with high robustness is needed to interface sub threshold circuit parts with above threshold module.

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II. CONVENTIONAL LEVEL SHIFTERS

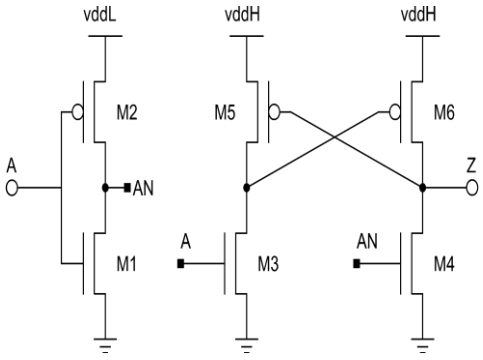

Fig.1.Conventional half latch- based level shifter

Fig.1. shows the basic level shifter [1]. A and AN are low voltage signals which is connected to the gates of M3 and M4 transistors.M5 and M6 forms a half –latch.M3 and M4 should be able to overcome the drive strength of PMOS transistors M5 and M6 when input is given. This can be achieved by sizing the NMOS transistor. As the voltage at M3 and M4 enters sub threshold regime, NMOS to PMOS ratio grows exponentially. This is because pull down transistor only allow a sub threshold on current while the pull up half latch has above threshold drive. For 90nm technology, NMOS to PMOS ratio required is N2400 and supply voltage of 200mv for operation. But due to large width of the NMOS transistor, this half latch LS is not suitable for sub threshold to above threshold level shifting.

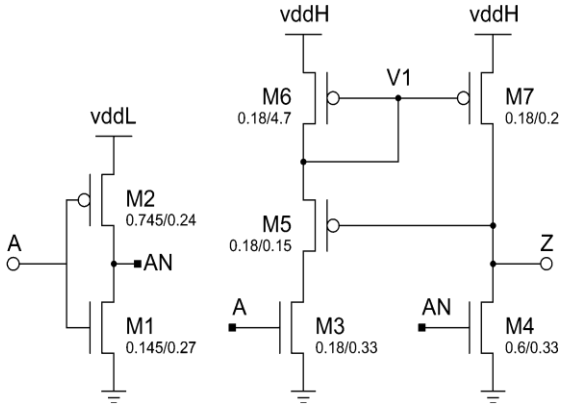

Fig.2 Wilson current mirror circuit

Wilson current mirror circuit [6] is shown in Fig.2.transistos M3 to M7 is the principal part of the circuit. A PMOS transistor M5 and M7 forms a current mirror. This M5 and M7 operates in it's over drive voltage. This circuit ensures that no current flows through M3 or M4 transistors when it is in off condition. When A is low & AN is high, M4 conducts(ON) which results in low Z.As A is low M3 is off and V1 gets charged through M6 until M6&M7 are low. When A is high & AN is low, M3 conducts(ON) which results in current flow through M3,M5,M6.Since M6&M7 are current mirror the current in M6 will also flows through M7.This current through M7 will charges Z. Thus when Z rises transistor M5 can be turned off to avoid static current through M3,M5,M6.This LS has better speed and performance but when the input voltage is high the output will floats. This causes destructive effect on sub threshold leakage of the output buffer.

The LS proposed in [1] have better transition from lower voltage to higher voltage. But this transition takes placed by deciding current driving capability of the pull down transistors. The LS proposed in [7] is a four stage cascaded DCVS circuit. It has better level up transition from the sub threshold regime. But unfortunately, it introduces large power consumption owing to the intermediate power supplies. Also it has a limited speed performance.

The LS proposed in [7] have two stages. The first stage exploits a DCVS circuit with an always on diode connected NMOS transistor on the top; whereas the second one is a conventional DCVS stage that achieves rail to rail swing. Such a design will avoids intermediate power lines but again it is not enough to reach high speed performances.

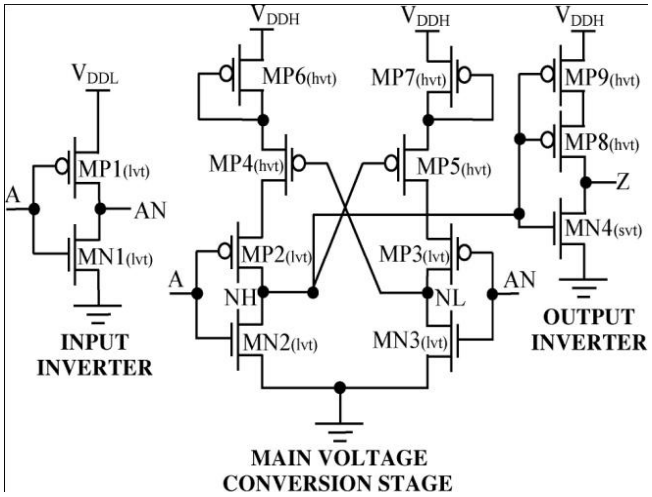

Fig.3 Multi supply voltage level shifter circuit

Fig.3 shows the multisupply voltage level shifter circuit [10]. The circuit consist of input inverter,voltage conversion stage and a output buffer. To provide fast differential low-voltage input signals, the input inverter was created using lvt devices. To increase the strength of the pull-down network of the main voltage conversion stage, it was also designed by using lvt transistors. The cross-bar current flowing through the nodes NH and NL at the beginning of their high to low transition [13] could be of concern. Thus, to reduce this effect, two lvt PMOS devices (MP2 and MP3) are adopted. MP4 and MP5 were chosen as hvt transistors. This helps in weakening the pull-up networks of the main voltage conversion stage, thus reducing contention at NH and NL nodes. This choice also reduces the leakage current flowing through the pull-up networks when they are turned off. Finally, to ensure reliable voltage conversion, two diode-connected hvt PMOS devices (MP6 and MP7) were placed between the pull-up logics and the supply rail VDDH. These devices limit the pull-up strength, but also lead to considerable reduced static power. A high to low transition of the main input causes MP4 being turned on. Its drain current brings the diode-connected MP6 device into the saturation region. This creates a voltage drop (i.e., Vth,MP6) across MP6 terminals that produces a correspondent bulk-source voltage drop on MP4. Due to the bulk effect, this increases the MP4 threshold voltage. The reduced voltage level (VDDH-Vth,MP6) on the source terminal of MP4 limits its VGS, thus further weakening the MP4 action. All the above effects reduce the contention on the node NH, thus allowing faster discharging to be achieved. When MP4 is turned on, MP5 is consequently turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 on. For this reason, MP5 results power gated from the VDDH power rail, leading to a

significant reduction in its sub-threshold current. The diode-connected MP7 device participates in minimizing the leakage current, also by increasing the threshold voltage of MP5. In fact, MP7 causes the source of transistor M5 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect.

The LS is suitable for up conversion from near/sub threshold regime. Also this circuit exhibits a very low static and dynamic energy consumption .But this system is obtained at the expense of reduced voltage conversion range and also it has limited speed. The proposed system is designed to reduce the above drawbacks.

III.PROPOSED LEVEL SHIFTER

The proposed level shifter circuit combines the multi threshold cmos design technique along with novel topological strategies. The input inverter (MP1/MN1) is designed using low threshold voltage (lvt) transistors. This provides fast differential low-voltage input signals to the main voltage conversion stage [10]. To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP2 and MP3) are added to both the branches of the circuit.

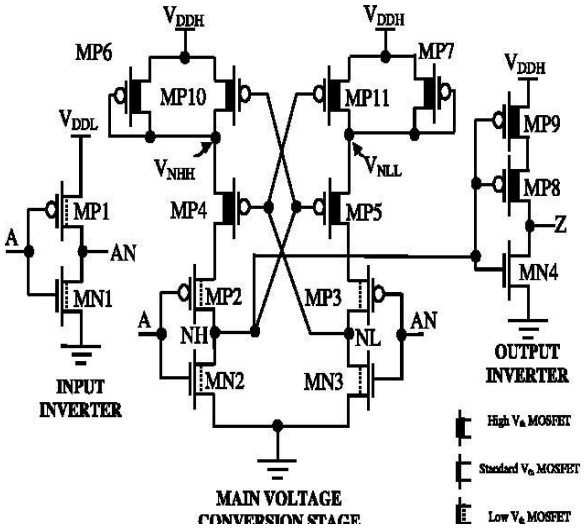

Fig .4 Novel low power level shifter circuit

To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP2 and MP3) are added to both the branches of the circuit. These devices limit the cross-bar current [11] that is the current flowing in the pull-up network and opposing to the discharge of NH (or NL) node at the beginning of their high to low transition. To further facilitate the high to low transition at the nodes NH and NL, MP4 and MP5 are high threshold voltage (hvt) transistors. This choice also reduces leakage current flowing through the pull-up networks when MP4 or MP5 are turned off. However, using hvt, pMOS transistors has the counter effect of slowing the low to high transition of the nodes NH and NL. Therefore, to reduce the switching delay, a pull-up network able to self-adapt its strength to the actually occurring transition would be desirable. This behavior was obtained by introducing the parallel connected hvt devices MP6-MP10 and MP7-MP11, with MP6 and MP7 being diode connected transistors. The latter devices impose two variable virtual power supplies VNHH and VNLL on the two branches of the circuit. Therefore, the strength of pull-up networks is adapted to the next output switching transition. That is, assuming that the output Z is initially low (high), the pull-up

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network of the left branch is weakened (strengthened) and that of the right branch is strengthened (weakened), thus speeding-up a low-to-high (high-to-low) output transition. The introduction of hvt MP10 and MP11 devices controlled by NH and NL voltages represents a significant difference with respect to the circuit previously proposed in [10]. . The proposed LS was designed using the 90-nm CMOS technology. The proposed level shifter has better speed compared to the previous systems. Also the power consumption is reduced without making any change in the systems function.

IV .RESULTS

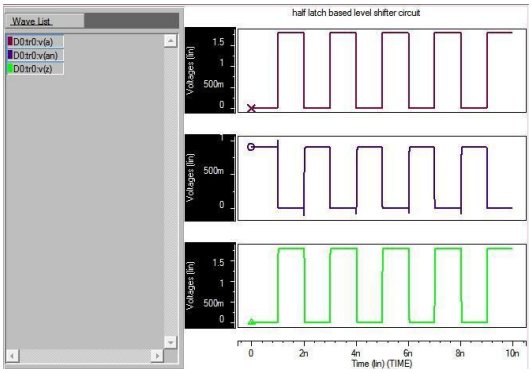

Fig .5. Waveform of Half latch level shifter

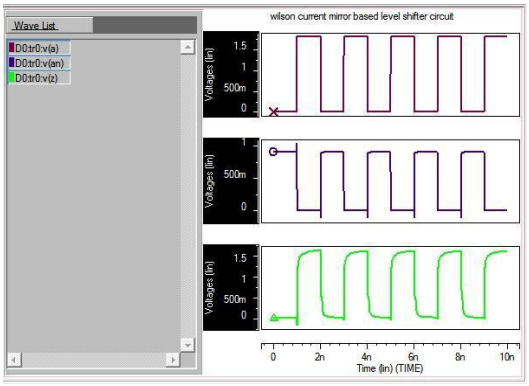

Fig.6. Waveform of Wilson current mirror LS circuit

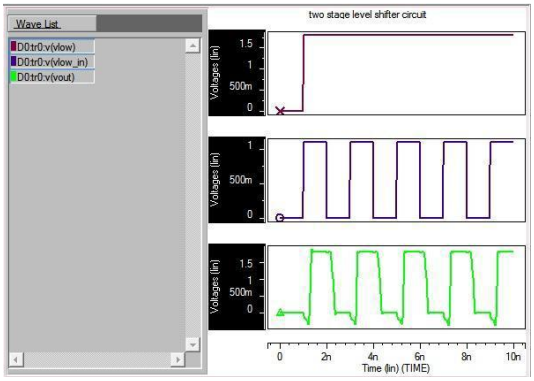

Fig.7. Waveform of two stage level shifter

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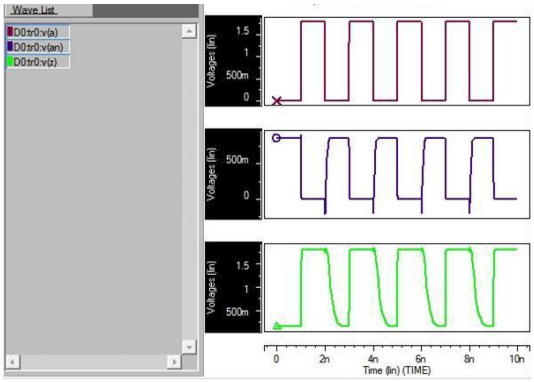

Fig .8. Wave form of Level Shifter with Multi Supply Voltage

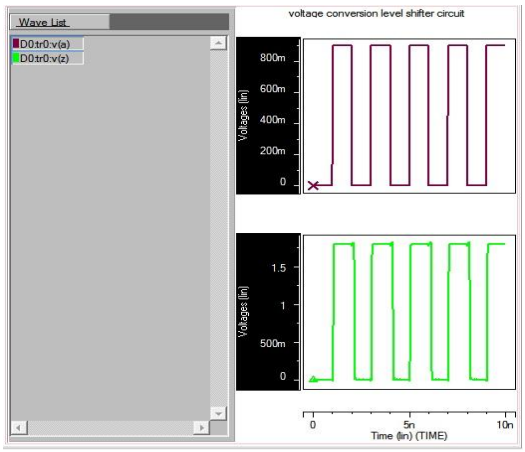

Fig .9. Waveform Of Proposed Low Power Level Shifter

Table .1. Result for half latch level shifter

S.No.	System	Delay(ns)	Power(µw)	PDP(FJ)
1	Half latch level shifter circuit	1.029	47.18	48.60

Table.2. Result for various level shifters

S.NO	Systems	Delay(ns)	Power(µw)	PDP(FJ)
1	Wilson current mirror LS circuit	1.058	272	288
2	Two stage LS circuit	1.319	223	295
3	LS circuit with multi supply voltage	1.35	209	282
4	Proposed system	1.156	65.97	58.24

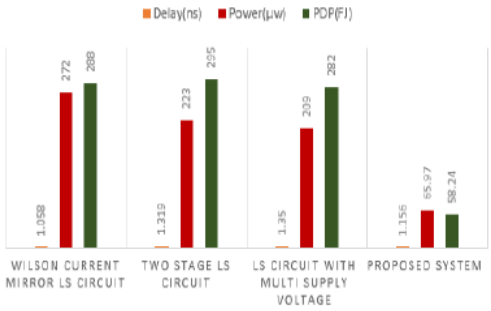

Fig.10. Power,Delay and PDP chart for various level shifter

V. CONCLUSION

Tthe level shifter that consumes low power was designed and implemented by using 90nm CMOS technology and simulated using HSPICE simulator.Finally results were compared with the existing systems. In order to improve the performance futher CMOS Technology can be replaced with FINFET.

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