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AN APPROACH TO PERFORMANCE CHARACTERISTICS OF SWCNT VLSI INTERCONNECTS SPECIFIC TO 22NM TECHNOLOGY NODE

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ABSTRACT

Single wall carbon nanotubes (SWCNTs) holds extremely good electrical and mechanical properties in conjugation to their application in sub nanometer regime and a viable replacement to Cu interconnects. This indeed raises a need to realize their Performance Characteristics which validates their potential application as VLSI interconnect. The paper intends to discuss an approach to performance characteristics of SWCNT VLSI Interconnects specific to 22nm technology node.

Keywords: Characteristicimpedance,50% Delay, Frequency Analysis, SWCNT Bundle, Transient Analysis,

I. INTRODUCTION

The present scenario of modern high speed, high density CMOS VLSI circuits aim at decreasing feature size along with increasing chip dimensions which results in increased complexity.The problem cannot be ignored as faster, dynamic and minimal circuits which consume least of power without compromising on their functionality are desired.

As we move towards deep submicron regime more no of interconnections are used to connect millions of devices. Thus resistance of wire increase significantly giving rise to propagation delay [4]. Earlier Al & Cu interconnects were viable enough, but the shrinking of device dimensions caused these conventional interconnects to suffer from problems like high electromigration resistance, surface roughness, grain boundary scattering, interconnect scaling, multiple interconnect stacks, leakage power, support to FinFET. Tang et al. [1] found that the continuous decrement in the feature size has brought to the arrival of certain problems like signal integrity, delay, crosstalk, rise time, high contact resistance and high processing temperature at a much significant level in comparison with the past.

The sub100 nm regime subjects increasing challenges for both active and passive components on the chip. The continuous scaling of the feature sizes of transistors and interconnects, increase in transistor speed, propagation delays, increment in contact resistance etc. have become the dominant chip performance limiting factor [2].

The above mentioned aspects of current technology advancements have carved a niche for a more convincing interconnect material which may withstand the ever-increasing performance requirements of interconnects in nanometer regime.

Consequently, materials such as carbon nanotubes (CNTs), graphene, nanoribbons, and Ag nanowires are being considered as potential replacements for Cu in interconnects, due to their better electrical and mechanical properties [3]. CNT appears to be a promising alternate to replace Cu due to its ultrahigh current capacity and it's filling ability in high aspect ratio structures.

The present paper aims to find an approach to performance characteristics of CNT VLSI interconnects specific to 22nm technology node. Various strategies followed to overcome problems with respect to the use of Carbon nanotubes are to be considered and authenticated with respect to 22nm technology node. It should also aims to validate the performance characteristics of mSWCNT in-particular as a possible replacement of conventional interconnect material.

II. MOTIVATION

In recent times CMOS processes are scaled down to nanometer regime. Though, scaling is of prime concern for VLSI design, it has given rise to new problems particularly for interconnects. These includes problems like electro migration, increased resistivity, lithography limitations and the speed/delay of the copper interconnect leading to find alternate interconnects. Consequently, alternate materials are envisaged for on-chip interconnects. This had lead us to gradual transition from Aluminium to Copper and presently Carbon-nano tubes (CNTs) and Graphene nanoribbons (GNRs) have emerged as a potential candidate to repudiate copper interconnects because of their enraged transport and ability to carry large current densities neglecting the effect of electro migration. Moreover, they provide extremely desirable properties of high mechanical strength, thermal stability and high thermal conductivity which is mandatory in case of interconnects. The research should initiate an approach to evaluate the potential use of CNTs as interconnects in IC design. It should focus on the relative interconnect delay, crosstalk, parasitic and power dissipation compared to the conventional interconnect materials such as Al & Cu and contemporary materials such as GNR,MWCNT,DWCNT and Optical Interconnects as with increment in the interconnect layers much investment is not preferred in raising the lithography expenditure. That's one reason, scaling is not preferred as in past.

The resistance of copper interconnects, with extremely low cross-sectional dimensions in current and forthcoming technologies is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of highly resistive diffusion barrier layer [6]. The steep rise in parasitic resistance of copper interconnects poses serious problems for interconnect delay especially when wire traverses long distances. Moreover, when a chip is connected to a board, there is unknown (potentially large) static voltage difference. Equalizing potentials requires (large) charge flow through the pads. Recently system on chip and embedded processors are used extensively, network on chip is the next technology [6]. Therefore, it is also equally important to find out suitable alternative material for interconnects for VLSI design.

III. STATEMENT OF THE PROBLEM

It is found that for a local wire, a CNT bundle displays a smaller latency than Cu for a given geometry [5]. In addition, by leveraging the superior electro migration properties of CNT and optimizing its geometry, the latency advantage can be amplified. In context to the proposed work, taking into consideration local, semi-global and global wires of commonly used elementary metrics: (latency, power dissipation and crosstalk), their improvised solution is to be found along with, a more judicial model of local semi-global and global interconnects. The above trends are to be scrutinised with respect to 22nm technology node. It should also be proposed to estimate and reduce the delay and energy expenditure for interconnect circuit schemes.

Interconnects utilised to connect various components present on the IC have the combined effect of parasitic resistance, capacitance and inductance associated with it. Each of the parasitic elements increase linearly with interconnect length .The increment of these parasitic elements give rise to unwanted coupling between the neighbouring lines thereby directly affecting signal integrity [7]. One of the prominent affects is the emerging of unwanted signal on the neighbouring lines known as crosstalk which is visible in terms of crosstalk voltage ($V_{crosstalk}$). This affect is elaborated with the help of Victim-Aggressor relationship possible solution for delay, unwanted spikes, and erroneous signals on the victim affecting its signal integrity are to be discussed.

On the basis of various models predicted, simulated and verified by various scientists it is concluded that CNTs application as VLSI Interconnects is one of the great possibilities to meet the ever demanding challenges of modern high speed, high density CMOS VLSI circuits which aim at decreasing feature size along with increasing chip dimensions. The limitations of crosstalk, glitches, signal integrity, spikes, logic levels, rise-time, grain boundary, MFP, electronmigration etc. which become more significant in nanometer and sub nanometer regime may be brought to limitations if conventional interconnect materials such as Cu/Al are convincingly replaced by carbon based possibilities such as SWCNT,DWCNT,MWCNT, GNR, MLGNR etc.

IV. PROPOSED CONCEPTUAL FRAMEWORK

Aim of the work should be to support the validity of mSWCNT as interconnect in nanometer range for local, semiglobal and global interconnects respectively. In doing so the complete performance analysis is aimed which commences at discussing the metallic nature of SWCNT to its authentication as an interconnect material. It should be also aimed to find the extent of crosstalk voltage in multiple aggressor environments with respect to interconnects of specific lengths and to provide methods to reduce the same. In doing so, the work intends to develop models for optimisation of interconnects in VLSI Circuits.

The work also needs to explore the possibility of applying the technique of repeater insertion and shielding to reduce crosstalk voltage, delay and power dissipation in interconnects. This includes the development of an analytical approach for optimum usage of repeaters and ground shielding for the reduction of crosstalk voltage, delay and power dissipation.

In due course a TLM model with DIL interface is considered where the following performance characteristics are analysed at 22nm technology node in specific.

1. Band Structure and Density of States Computational Analysis of mSWCNT for different Structural Parameters.

2. Characteristic Impedance and Parametric Variation effects on SWCNT bundle Interconnect at 22 nm Technology Node
3. Time Domain Analysis of Bundled SWCNT Interconnects at 22nm Technology node based on Transmission Line Model
4. Crosstalk prediction and estimation in Bundled SWCNT Interconnects at 22nm Technology node
5. Crosstalk reduction in Bundled SWCNT Interconnects through repeater insertion at 22nm Technology node

The following procedure is followed for achieving the same.

1. A transmission line model is proposed, based on lumped parameters using interconnect lengths with two aggressors and one victim line in between.
2. T-SPICE, HSPICE and MATLAB simulations are to be used for verification of the validity of the analytical method.
3. The extent of crosstalk voltage, delay and power dissipation needs to be estimated and compared by varying the interconnect lengths with respect to local, semiglobal and global interconnects.

The above mentioned problems are analysed and possible solutions have to be predicted based on the TLM model with DIL interface subjected to simulation tools mentioned below.

1. CNTBANDS
2. LTSPICE (IV)
3. TANNER TOOL (Ver.14)
4. MATLAB 8.5
5. HSPICE

These tools are convincingly used to predict the performance characteristics of mSWCNT bundle working as interconnects in nanometer regime, specifically 22nm technology node.

V. RESEARCH OUTLINE

The research should initiate by discussing the integrated circuit technology, VLSI interconnects and a prologue to various types of CNT interconnects. It also should aim at discussing various types of crosstalk that mitigate into the system and introduces significant errors.

An extensive paradigm should be envisaged to the literature review on CNT interconnects taking key- note on the modelling and simulation issues, of SWCNTs, MWCNTs, CNT vias and MCB interconnects ,models and theories formulated to justify the application of CNT as interconnect substitute to conventional interconnect materials.

The metallic nature's origin of Carbon nanotubes with emphasis on concepts like band structures of mSWCNT, density of states of mSWCNT and lowest subband p_z tight binding in mSWCNT needs to be addressed, including the dependence of metallic nature of SWCNT on chiral vector and other additional parameters contributed by the same.

Various formulae and theoretical concepts related to CNT as an isolated and bundled structure specifically for the modellingof MCB interconnects needs to be quantified, specifically catering to the realisation of mSWCNT as bundled interconnect. The study should also include the TLM and DIL system respective to various technology nodes which necessitates its presence as various performance characteristics of the system are based.

The characteristic impedance and parametric variation effects on SWCNT bundle interconnect at specific technology node should be included where, the characteristic impedance of SWCNT bundle interconnects geometries are proposed as a function of physical parameters such as length, diameter and frequency while authenticating against SPICE simulated results. Characteristic impedance variation, depicted as a function of diameter and length of interconnects at constant frequency with current model needs to be attended. The sole purpose of the same is to assist designers to realize compatible loading impedance for SWCNT bundle interconnects to reduce signal reflections and attenuations at minimum level. It is should also be aimed to estimate the range of frequencies that may be transmitted through interconnects at different lengths and diameters under critical mismatch conditions.

TLM of SWCNT bundled interconnect is included to obtain the time domain analysis of bundled swcnt interconnects at technology node based on transmission line model. The step response, frequency analysis along with bode stability and the suitability of the model with respect to Nyquist criterion supported with suitable illustrations and simulation results needs to be quantified. So far an authenticated model has been developed aiming at the utilisation of mSWCNT bundle as interconnect with respect to the optimised TLM incorporated with DIL system specific to 22nm technology node.

The interconnect dimensions ; including length and diametermay be varied with respect to local, semiglobal and global regimes and various step responses , Nyquist diagrams and Bode plots are generated to study the effect of mSWCNT geometry on the step responses and relative stability of interconnects.

More accurate analysis (i.e., the sixth order linear approximation), may be achieved by showing the Nyquist diagrams, demonstrated to obtain the relative stabilities with propagation delays, as mSWCNT's dimensions are varied [8].

Next, crosstalk is predicted and estimated in bundled SWCNT interconnects at 22nm technology node which solely decides the extent of noise in the present model. This in-turn not only validates the application of the model but also predicts the extent of disturbing noise which has an adverse effect in VLSI circuits of nanometer regime. In addition, the measures of reducing crosstalk effects that have emerged in the TLM of mSWCNT bundled interconnect is also estimated. This is achieved with repeater insertion at optimum lengths supported by analytical evaluation for, 50% delay, hopt, kopt, buffer size, τ_{delay}, minimum size repeater, optimum repeater interval, number of repeater, total delay

Finally, all the analytical, simulation results obtained are emphasised to validate the application of SWCNT bundled interconnect in nanometer regime that authenticate various strategies to be followed making interconnect compatible with the DIL system at specific technology node. The research should also aims to reports applications, benefits and various limitations of the proposed model. Future research directions also needs to be suggested for preceding researchers. The emerging applications and future of CNTs, also be discussed at a stretch.

VI. CONCLUSION

All the aspects discussed above may be visualized in fig.1 with an optimistic approach that the above stated strategies if followed may assist the researcher to completely realise and validate the performance characteristics of CNT VLSI Interconnects specific to 22nm technology node.

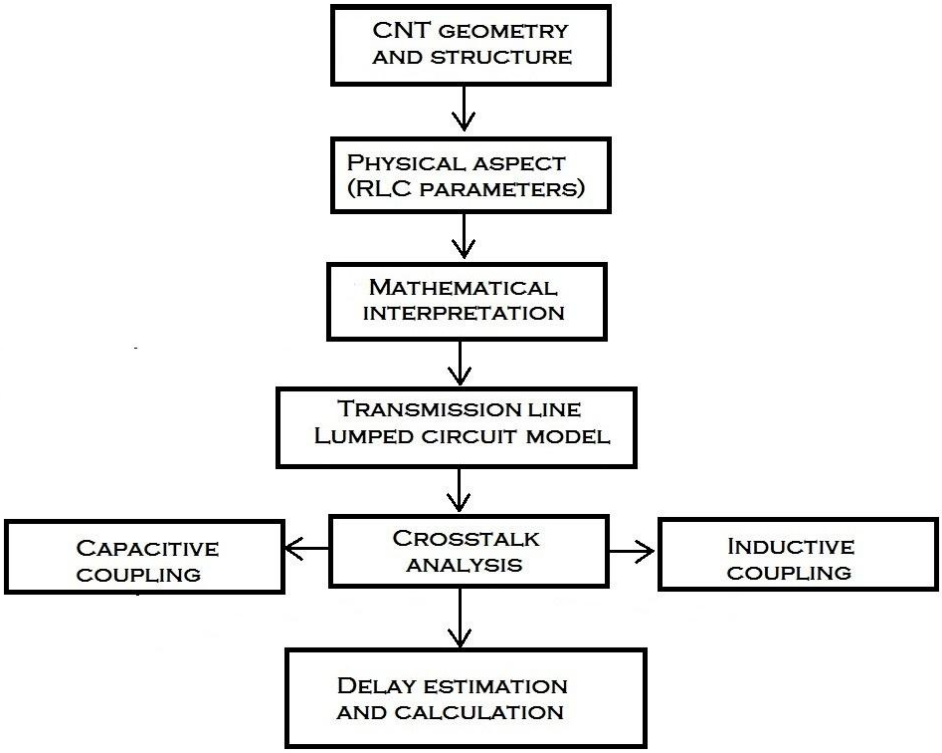

Fig.1: An approach to Performance Characteristics of CNT VLSI Interconnects specific to 22nm technology node

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