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VLSI DESIGN OF LOW POWER ADDER CIRCUIT AND ITS APPLICATIONS

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ABSTRACT

With the explosive growth in laptops, portable personal communication systems and the evolution of the shrinking technology low-power design can be addressed at different design levels, such as software, architectural, algorithmic, circuit, and process technology level . This paper presents an effective approach to reduce power consumption of any arbitrary combinational logic circuit by applying transformations at the logic level, whilst preserving the desired functionality. We have considered implementation with static CMOS logic style, due to its robustness against device and process variations. Simulation results obtained using a 0.180 micron TSMC CMOS technology for savings power by 25% over the best of existing methods; while considering spatio-temporal correlation in inputs, average power savings of 13.22 % was obtained. The proposed method also enabled overall improvement in worst case delay parameter by 26.52%, over the best of other methods.

Keywords: LSI; Majority Function; Combinational Logic;CMOS

I. INTRODUCTION

The research effort in low-power microelectronics has been intensified and low-power VLSI systems have emerged as highly in demand. Today, there is an increasing number of portable applications requiring small-area low-power high- throughput circuitry. Therefore, circuits with low power consumption become the major candidates [1–3] for design of microprocessors and system-components. The battery technology does not advance at the same rate as the microelectronics technology and there is a limited amount of power available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not necessarily imply low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation. Therefore, designers are faced with more constraints such as high speed, high throughput, and small silicon area and at the same time low power consumption. This is why building low- power, high-performance adder cells is of great interest.

Addition is one of the fundamental arithmetic operations and is used extensively in many VLSI systems. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. [4-21]. In most of these systems, the adder is part of the critical path that determines the overall performance of the system and the full adder is the core element of complex arithmetic circuits. That is why enhancing the performance of the 1-bit full-adder cell [17-

21] (the building block of the binary adder) is considered a significant goal. Lowering the supply voltage appears to be the most well- known means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. Recently, clustered voltage scaling and dual voltage supply schemes have been proposed to maintain the chip throughput by selectively lowering the supply voltage for noncritical sub-circuits [10, 11].

One of the objective of this work is to design a circuit based on 0.18 µm- CMOS process technology that can be operate at ultra low power supply voltage.

The rest of the paper is organized as follows Section II explores the review of majority function inverter and the NAND logic. The implementation of majority function full adder is proposed in Section III. In section IV the one bit full adder is simulated on 0.18 µm- CMOS process technology. Finally section V concludes the paper.

II. MAJORITY FUNCTION (MF)

In Boolean logic, shown in fig.1 and the truth table shown in table.1 is the majority function .A function from N- inputs to one output. The value of the operation is false when N/2 or more arguments are false, and true otherwise. Alternatively, representing true values as 1(logical high) and false values as 0(logical low).

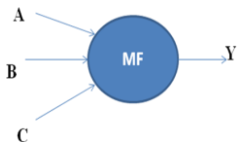

Figure 1 Majority Function

Table 1 Truth Table Majority Function

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The three-input majority not function is shown in Fig. 2and the corresponding waveforms shown in fig.3. In order to create this function, it uses three-input capacitors that prepare an input voltage for driving the CMOS inverter. The circuit shown in Fig. 4 working as a majority NAND function. The transistor sizing that shifts VTC in to the left and right through changing the ratio of (W/L)n to (W/L)p shown in fig.5 . Rising this ratio moves VTC into the left therefore this circuit will operate as an NOR function. In reverse, decreasing that ratio makes NAND function. Appropriate values for these parameters should be found in order to create the Majority

Not Function using this circuit. fig 3 shows the output waveforms of the circuit by changing the size of transistors. However, different functions are implemented with unique circuit and all of them can be designed by selecting correct values but in the presented full adder this circuit is only used as the Majority Not Function.

This method suffers from an excessive power dissipation caused by the short-circuit current in a steady state and also during transient from high to low and vice versa when both transistors are on.

This proposed method is based on high threshold voltages transistors [1,10–21]. For implementing the Majority Not Function by the circuit shown in Fig. 4, high-Vt transistors have been used. The NMOS transistor must be turned on (Vgs4 Vthn) and the output has to below when at least two out of the three inputs are high and vice versa while two or three of inputs are low. The threshold voltage of the PMOS and NMOS transistors are 0.48 and 0.47 V, respectively. This method has the benefit of a very low P direct path and the short-circuit current. The circuit also is a ratio less one and in addition the energy consumed per switching activity is better:

$$P_{tot} = P_{dyn} + P_{dp} + P_{state} \quad (1)$$

$$= CLVDD_2 + VDD_1 leak + (tr+tf/2) + VDD_l leak \quad (2)$$

(A) Majority NAND Function

A new design technique for NAND, NOR and MAJORITY-NOT gates proposed analyzes their performance and power consumption The circuit for implementing the universal gates is illustrated in Fig. 2. Because of just two transistors the supply voltage can be reduced. In this situation P short-circuit is eliminated due to Eq. (2),and because of low voltage scaling, Pdynamic is reduced in a quadratic manner. So the average power dissipation is lower than conventional CMOS gates.

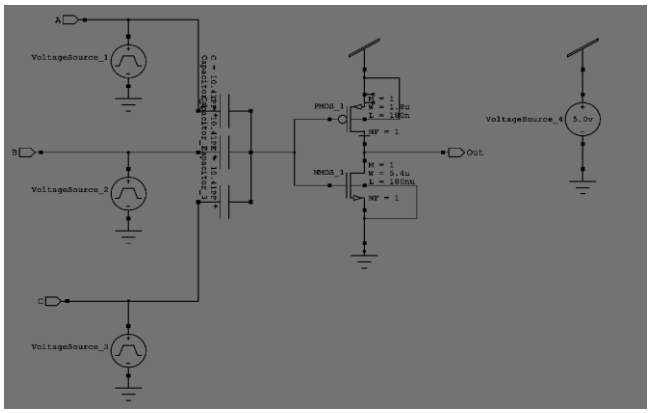

Figure 2 Three Input Majority NOT Function

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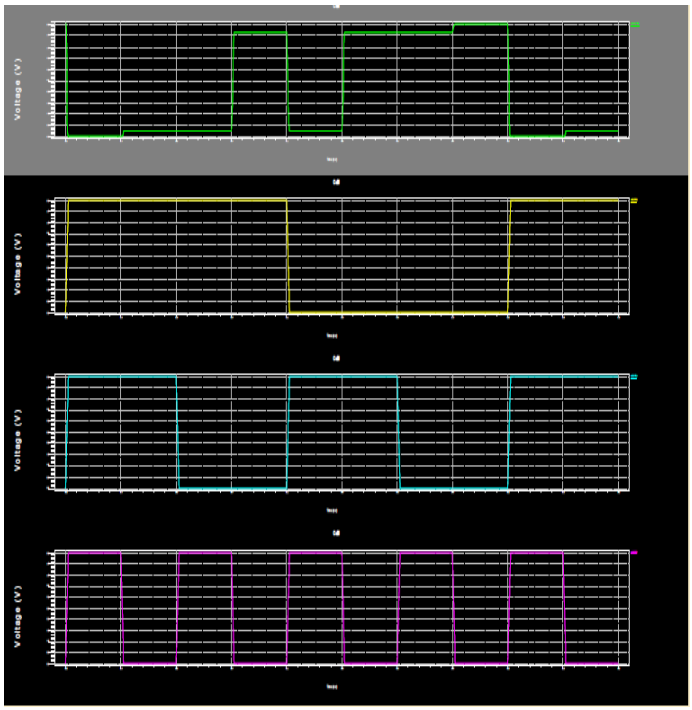

Figure 3 Wave Form of three Input Majority Function Inverter

To implement NAND Gate with Fig.4 it is just enough to use high -Vth NMOS and low- Vth PMOS finally in order to have MAJORITY-NOT Function both transistors are replaced with high-Vth transistors .Using high-threshold voltage transistors and low-threshold voltage transistors in addition to normal-threshold transistors have been accomplished in low- power application, and many circuits have enjoyed this technique in low-power design. Multi-threshold CMOS (MTCMOS) circuits and dual -Vth techniques use high-Vth transistors to eliminate and reduce the leakage current through a transistor, thereby decreasing leakage power consumption while maintaining performance

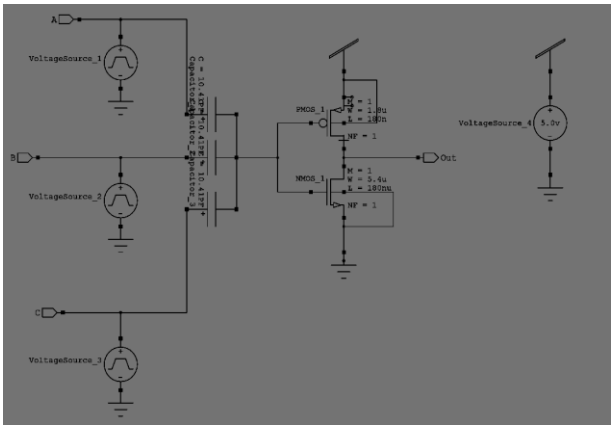

Figure 4 Majority Function NAND Gate

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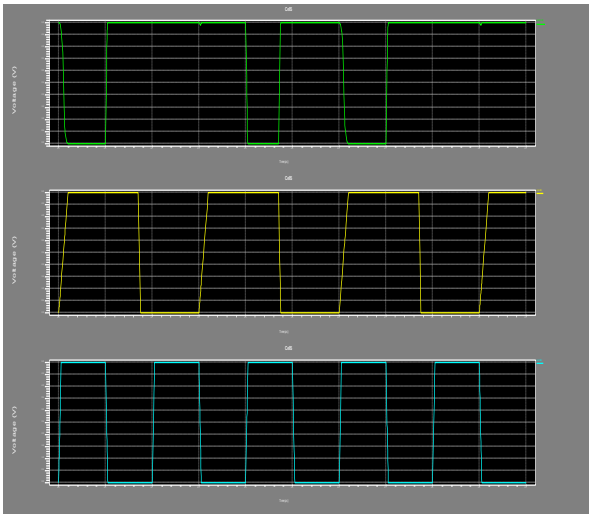

Figure 5 Waveform of Majority Function NANAD gate

III. IMPLEMENTATION OF MAJORITY FUNCTION FULL ADDER

Three input and the five input majority function have been used in the proposed adder. The full adder operation can be stated as follows: given the three inputs A, B and C. it is desired to calculate two one bit outputs, SUM and Cout. Table 2 shows the truth table of Cout, SUM and Three input majority function.

As the above table shown, Cout can be implemented with a three input majority function.

$$Cout = AB + AC + BC \qquad (3)$$

If we invert the output of the circuit, $\overline{Cout}$ is produced.

As table .2 exhibits SUM is different in merely two places with majority Not function; when inputs are 000 and 111. Therefore, SUM can be calculated with $\overline{Cout}$ as shown in equ (4) . Fig 8.showns the one bit adder circuit using majority function logic and the simulation results are shown in fig.9 and fig. 10.

Table 2 Truth Table of Majority Function Full Adder

A	B	C	Cout	SUM	MF	Not(MF)
0	0	0	0	0	0	1
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	1	1	0

$$SUM = ABC + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= ABC + (\bar{A}\bar{B}.\bar{A}\bar{C}.\bar{B}\bar{C}) + (A+B+C)$$

$$= ABC + \overline{Cout}.Cout + \overline{Cout}(A+B+C)$$

$$= ABC + \overline{Cout} + (AB + AC + BC) + \overline{Cout}(A+B+C)$$

$$= \text{Majority}(A, B, C, \overline{Cout}, \overline{Cout}) \qquad (4)$$

Consequently, according to this fact, SUM is generated by means of two majority Not function as illustrated in Fig.7.

The first one is a three input majority Not function that makes $\overline{Cout}$ and the second one is a five input majority function which creates SUM.

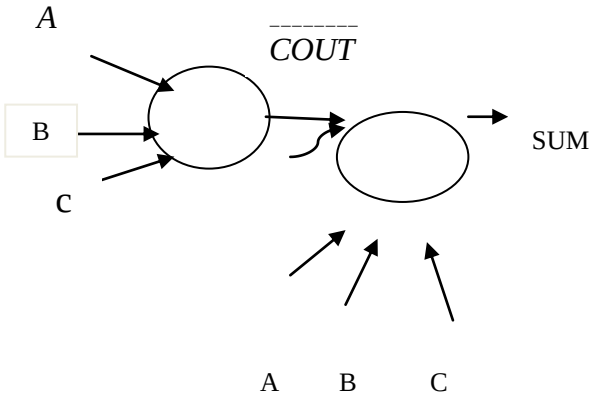

Figure 6 Majority Function based Full Adder

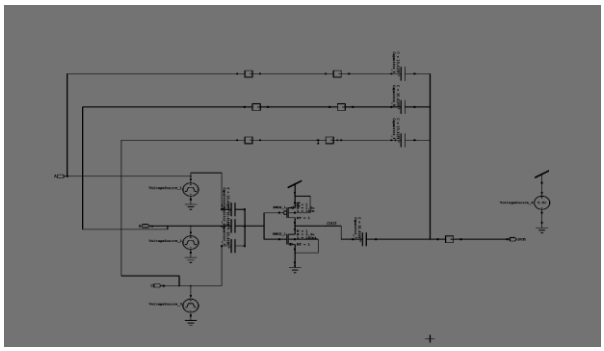

Figure 7 Majority Function Based Full Adder

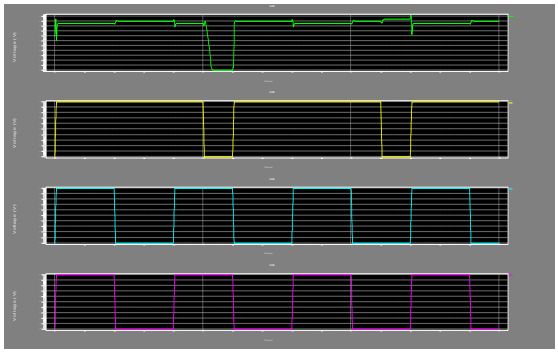

Figure 8 Waveforms of SUM

IV. SIMULATION RESULTS

The proposed adder has been simulated on tanner EDA by using).18 µm technology. The threshold voltage of the NMOS and PMOS transistors are around 0.45 and -0.35 V but the proposed adder uses the high Vt transistor with 0.47 and -0.48 V by optimizing the transistor sizes of full adders considered. It is possible to reduce the delay of the adders without significantly increasing the power consumption and the transistor sizes can be set to achieve the minimum power delay product (PDP).

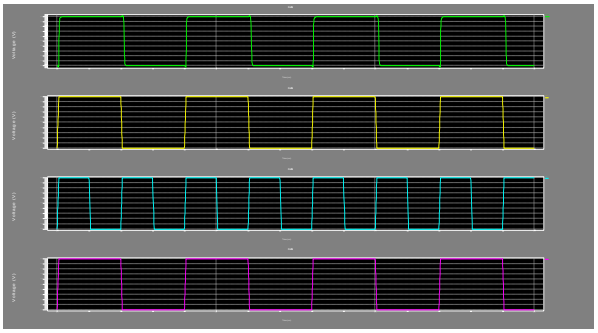

Figure 9 Waveforms of Cout

V. CONCLUSION

In addition to the discussion which result in having an acceptable penalty in area due to improvement in manufacturing and implementation of capacitors more compatible capacitors with high capacitance value have been made. These new capacitors got their high capacitance value by reduction in the thickness of their oxide so the conclusion is that as the capacitor with compact size are implemented with a little increase in length of the channel.

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