International Journal of Electrical and Electronics Engineers
Vol. No.7 Issue 02, July-December 2015
www.arresearchpublication.com
IJEEE ISSN 2321 - 2055

SPMC OPERATING AS A FREQUENCY CHANGER BASED ON FPGA

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ABSTRACT

In this paper a Sinusoidal Pulse Width Modulation (SPWM) technique is used to synthesize the output voltage with increased frequency. The power circuit uses Insulated Gate Bipolar Transistor (IGBT) as switching device in implementation. This paper is using Field Programmable Gate Array (FPGA) design for control implementations of the Single-Phase Matrix Converter (SPMC) operating as a Frequency Changer.

Keywords: Sinusoidal Pulse Width Modulation (SPWM), Single-Phase Matrix Converter (SPMC), Field Programmable Gate Array (FPGA), Cycloconverter, Very high speed integrated circuit Hardware Description Language (VHDL)

I. INTRODUCTION

Matrix Converter (MC) is a converter known to offer an "all silicon" solution for direct AC-AC conversion [1, 2], mainly with three-phase circuit topologies [3]. The single-phase version has subsequently been investigated called the Single-phase Matrix Converter (SPMC) for AC-AC conversion [4, 5, 6]. Limited publications had been found on SPMC, definitely negligible on switching strategies due to complex control requirements with its four bidirectional switch topology and the absence of simple safe commutation strategy [7]. Pulse width modulation (PWM) is a widely used technique for controlling the output of static power converters. They have different implementations, dynamics responses and PWM patterns [8].

The design and development of a sinusoidal pulse- width modulation (PWM) generator suitable for Single-Phase Matrix Converter (SPMC) operating as a frequency changer will be presented. It is based on the Xilinx chip XC4005XL Field Programmable Gate Array (FPGA) with IGBTs as the power switching device. The output voltage is synthesized using Sinusoidal Pulse Width Modulation (SPWM). The proposed design enables the modulation index and the switching frequency to be changed externally. Results are provided to demonstrate successful implementation of the design. Prior to hardware implementation, simulations were performed to predict the behaviour.

II. XILINX FPGA DESIGN

The functional block diagram of control algorithm developed for implementation of Xilinx to produce switching pattern for SPMC operating as cycloconverter is as shown in Figure. Within the Xilinx is three major components; a) Desired Output Frequency (DOF), b) Switch Selector Unit (SSU) and c) Commutation Switch

Selector (CSS). The SPWM algorithm is converted into a digital form as illustrated in Figure. Due to their similarity nature of the sine-wave between the negative and positive cycle; a half cycle (positive) could be used to optimise by repeating it in the negative cycle; performing required functions but at reduced overheads.

Before the advent of programmable logic, custom logic circuits were built at the board level using standard components, or at the gate level in expensive application-specific (custom) integrated circuits. The FPGA is an integrated circuit that contains many (64 to over 10,000) identical logic cells that can be viewed as standard components. Each logic cell can independently take on any one of a limited set of personalities. The individual cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix. The array of logic cells and interconnects form a fabric of basic building blocks for logic circuits. Complex designs are created by combining these basic blocks to create the desired circuit. The FPGA's function is defined by a user's program rather than by the manufacturer of the device. A typical integrated circuit performs a particular function defined at the time of manufacture. In contrast, the FPGA's function is defined by a program written by someone other than the device manufacturer. Depending on the particular device, the program is either 'burned' in permanently or semi-permanently as part of a board assembly process, or is loaded from an external memory each time the device is powered up. This user programmability gives the user access to complex integrated designs without the high engineering costs associated with application specific integrated circuits.

With successively improving reliability and performance of digital controllers, the digital control techniques have predominated over other analog counter parts. There are many advantages of digital controllers are such as reconfigurability, power saving options, less external passive components and less sensitive to temperature variation.

III. FREQUENCY CHANGER

A classical rectifier-inverter system that could perform frequency conversion can be depicted as shown in Figure 1, where the use of storage device for the DC link is necessary for operation. A direct AC-AC converter on the other hand converts a fixed frequency fixed voltage input into a variable frequency variable voltage output without the use of intermediate storage device. Increased frequency operation of AC-AC conversion can be illustrated ideally as shown in Fig. 2 and maybe implemented using direct AC-AC converter for electronic transformer operation [9], adjustable speed drives [10] , induction heating or other applications.

International Journal of Electrical and Electronics Engineers
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www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

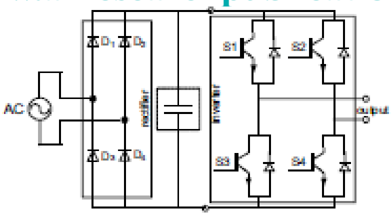
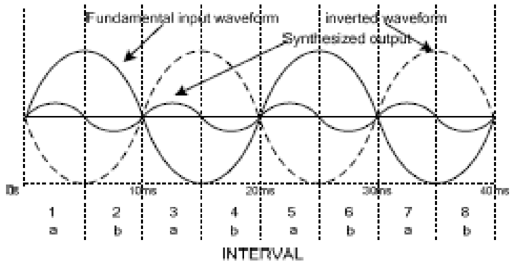
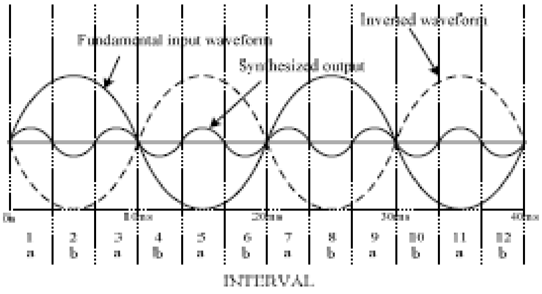


Fig. 1: Classical Rectifier-Inverter AC-AC Converter



(a)



(b)

Fig. 2: Increased Frequency Operation (a) 100 Hz (b) 150 Hz

IV. SINGLE-PHASE MATRIX CONVERTER

The SPMC topology with its 4 bi-directional switches and its individual power switches; used in this work is as shown in Figs. 3 and 4 respectively; each capable of conducting current in both directions, blocking forward and reverse voltages [7] with the associated safe commutation switching sequence as illustrated in Figs. 5 to 8 is used. These avoid the occurrence of switching transients relating to use of reactive loads available during switch turn-off and commutation. To synthesize a variable voltage output the SPWM as illustrated in Fig. 9 is used. The switching sequence for operation of SPMC as the frequency changer with increases in frequency from an input of 50Hz to an output of 100Hz and 150Hz is tabulated in table with its associated illustrations as shown in Figs. 10.

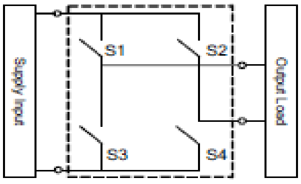


Fig. 3: SPMC circuit configuration

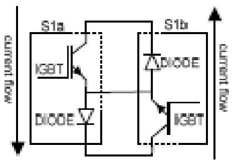


Fig.4: Bi-directional switch module

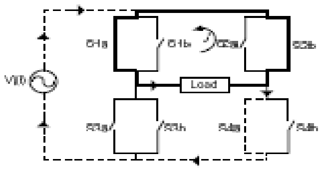


Fig. 5: Positive Cycle (State 1)

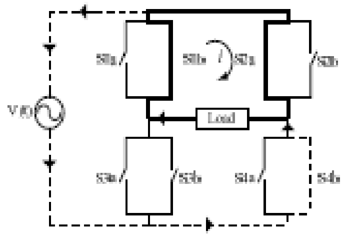


Fig.6: Negative Cycle (State 2)

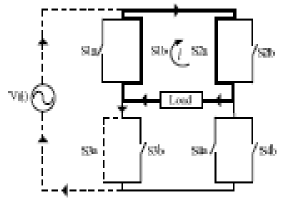


Fig. 7: Positive Cycle (State 3)

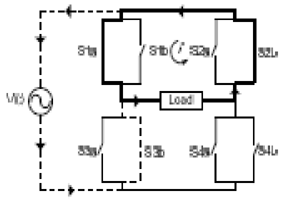


Fig. 8: Negative Cycle (State 4)

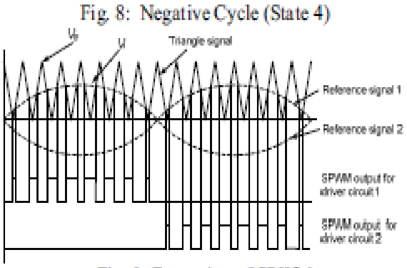


Fig. 9: Formation of SPWM

SEQUENCE OF SWITCHING CONTROL

Input Frequency	Output Frequency	Time Interval	State	PWM Switch	Commutation Switch
50 Hz	50 Hz	1	1	S4a	S1a & S2b
		2	2	S4b	S1b & S2a
	100 Hz	1	1	S4a	S1a & S2b
		2	3	S3a	S1b & S2a
		3	4	S3b	S1a & S2b
		4	2	S4b	S1b & S2a
	150 Hz	1	1	S4a	S1a & S2b
		2	3	S3a	S1b & S2a
		3	1	S4a	S1a & S2b
		4	2	S4b	S1b & S2a
		5	4	S3b	S1a & S2b
		6	2	S4b	S1b & S2a

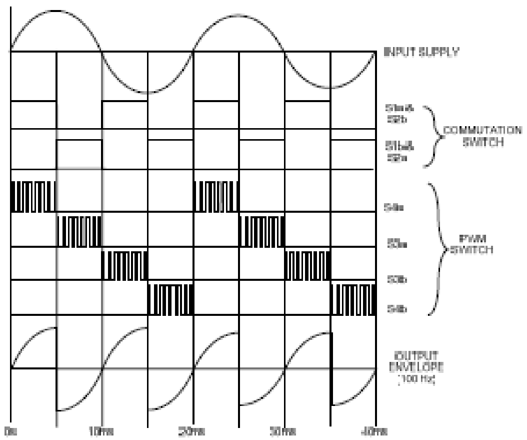


Figure 10 (a)

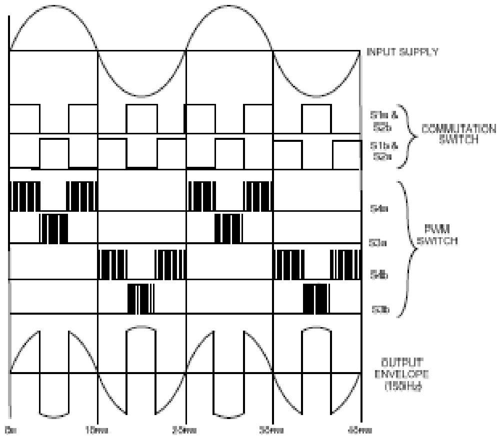


Figure 10 (b)

Figure 10 : Switching illustration (a)100 Hz (b)150 Hz

V. CONCLUSION

Experience in designing the FPGA for implementation of frequency changer using matrix converter has been presented. It has been shown that the FPGA could effectively be used in SPMC control with the four bidirectional switching arrangements. The overall system is compact with no external memory system required.

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IJEEE
ISSN 2321 - 2055

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