DESIGN OF LOW POWER MULTIPLIER USING REVERSIBLE LOGIC GATE

Mr. Ashish K. Thakre[1], Mr. Jagadish S. Rokde[2]

[1, 2] *Lecturer, Electronics Engg. Department, Shri Datta Meghe Polytechnic, Nagpur, (India)*

ABSTRACT

The reversible logic has received great attention in last few years due to their ability to decrease the power dissipation which is the main requirement in low power VLSI design. The traditional set of gates like AND, OR and EXOR are not reversible. This paper proposes a 4x4 bit reversible multiplier circuit using Peres gate which can multiply two 4- bit numbers. It is faster and has low hardware complexity compared to the existing designs. In addition, this reversible multiplier is better than the existing counterparts in terms of delay and power because the Peres gate reduces the garbage output. It is based on the two concepts, The partial products can be generated in parallel using Peres gates and thereafter the addition is done of all product terms by using reversible parallel adder designed from TSG gates. After that we replace the reversible parallel adder by modified reversible adder then we compare both the multiplier and compare the terms like garbage outputs, power dissipation, number of gates required and number of constant inputs. Thus, this paper provides the comparison of two multipliers according to their garbage outputs, power dissipation, number of gates required and number of constant inputs.

Keywords - Reversible Logic, Reversible Gate, Power Dissipation, Garbage.

I. INTRODUCTION

It is a well known fact that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur if the computation were carried out in a reversible manner [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system consists of reversible gates. In reversible logic there is one-to-one mapping between the input and output vectors and vice-versa. Reversible logic is likely to be in demand in high speed power aware circuits, low-power CMOS design, optical computing, nanotechnology and quantum computing. The sequential logic differs from combinational logic in that the output of the logic device is dependent not only on the present inputs to the device, but also on the past inputs. This paper provides a step to building more complex reversible systems by introducing the novel designs of reversible sequential circuits. One of the major goals in reversible logic design is to minimize the number of reversible gates and garbage outputs (garbage outputs are the unutilized outputs required to maintain reversibility). In this work, we are proposing the reversible designs of latches and flip flops. The proposed designs are shown to be better than the existing designs in terms of number of reversible gates and garbage outputs. There are a number of existing gates in literature. But in our proposed designs, we

have basically utilized the three reversible gates, viz., Fredkin Gate, Feynman gate and Toffoli gate [3, 4]. Twonew reversible gates termed modified Toffoli gate (MTG) and modified Fredkin gate (MFG) are also proposed keeping the goal of minimization of number of reversible gates and garbage outputs in mind. The transistor implementations of the existing as well as the newly proposed gates are also shown. Thus, our proposed reversible sequential designs are practically feasible to implement in silicon technology.   To the best of our knowledge, this is the first work to propose the feasibility of transistor implementation of reversible sequential circuits designed using reversible gates. The recently proposed work in this area [7] builds the reversible RS latch and then introduces the reversible flip flops designs based on the reversible latch implementation. In the proposed work, we have compared our work with that proposed in [7]. The paper is organized as follows. Section II deals with the basic reversible gates and their transistor implementations. Section III & IV shows the proposed reversible designs of latches and flip flops, respectively. Section VI provides the conclusions.

II. BASIC REVERSIBLE GATES AND PROPOSED TRANSISTOR IMPLEMENTATION

This section deals with the description and transistor implementation of existing as well as newly proposed reversible gates, utilized in designing the proposed reversible sequential circuits.

A. Feynman Gate

Feynman gate [3,4] is a 2*2 one-through reversible gate shown in Fig. 1. One through gate means that one input variable is also the output.
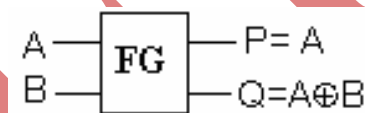

Fig. 1. Feynman Gate

2.1 Proposed Transistor Implementation

Fig. 2 shows the proposed transistor implementation of the Feynman gate. The proposed transistor implementation is completely reversible, that is, the proposed circuit can also work for reverse operation.
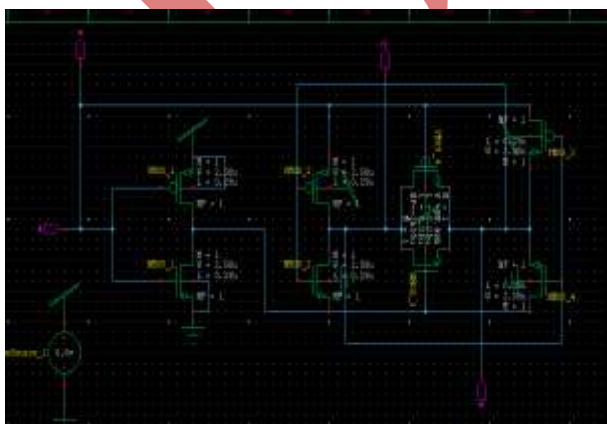

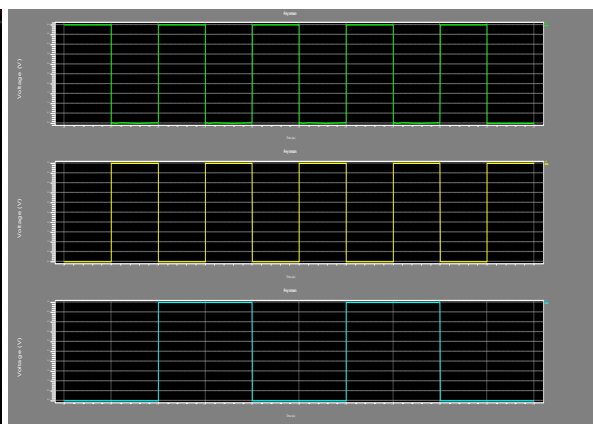**Fig. 2. Reversible Transistor Implementation Of The Feynman Gate**

Fig. 3. W a v e f o r m s O f Reversible Transistor Implementation Of The   Feynman Gate

In other words, we can calculate the *forward calculation*

P=A, If A=0 then Q=B

 Else Q=B'

as well as the *reverse calculation*

A=P;

If P=0 then   B=Q Else B=Q'

 As depicted in Fig. 2, 8 transistors are needed to design the fully reversible Feynman gate. The existing approach in literature also takes 8 transistors and is based on dual rail logic pass transistor logic [6]. Thus, our approach should be regarded as an example of new methodology of providing the transistor implementation of reversible logic gates. The proposed approach will reduce the number of transistors required to design Fredkin and Toffoli gate as discussed in next sections.

B. Fredkin Gate

Fredkin gate is a (3*3) conservative reversible gate [3,4] as shown in Fig.4. It is called 3*3 gate as it has three inputs and three out- puts.
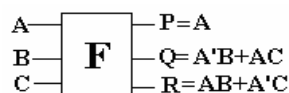

A— [F] —P=A

B— —Q=A'B+AC

C— —R=AB+A'C

Fig. 4. Fredkin Gate

2.2 Proposed Transistor Implementation Of Fredkin Gate

 Fig. 4 shows the proposed transistor implementation of the Fredkin Gate which requires only 4 transistors. In the proposed implementation, the output P is directly taken from input A as it is simply hardwired. The existing implementation of the Fredkin gate in literature is with 10 transistors [5] and 16 transistors [6] respectively. Thus proposed design achieves 60% reduction in number of transistors compared to [5] and 75% reduction compared to [6]. Noted that our proposed transistor implementation is suitable both for forward as well as backward computation, i.e., completely reversible in nature. The forward and backward computations for Fredkin gate are explained below.

Forward Computation:

$$P=A$$

If A=0 then Q=B and

$$R=C,$$

Else   Q=C and R=B

Backward Computation:

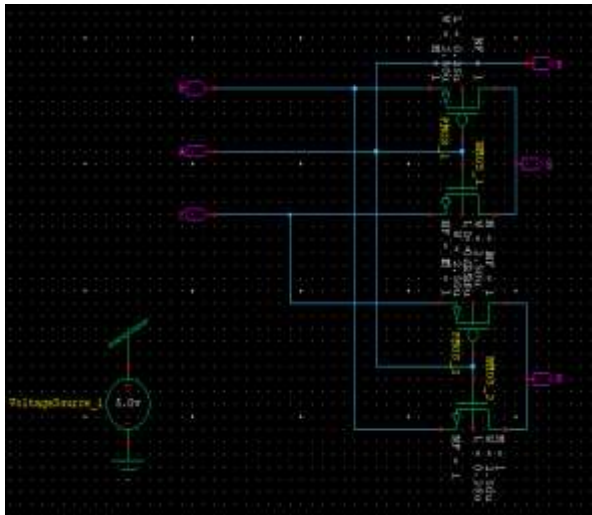 A=P If P=0 then B=Q and

            C=R

      Else C=Q and B=R

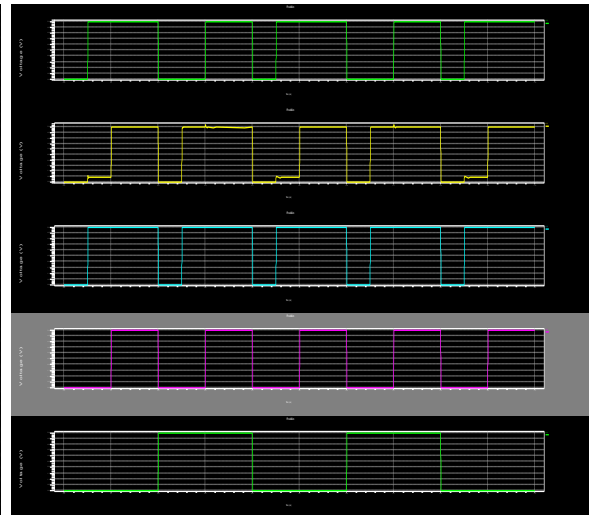**Fig. 5. Reversible Transistor Implementation   Fig. 6. Waveforms Of Reversible Transistor**

Of The Fredkin Gate   Implementation   Of The Fredkin Gate

C. Toffoli Gate

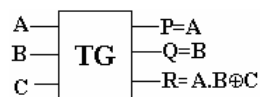Toffoli Gate (TG)[3, 4] is a 3*3 two- through reversible gate as shown in Fig. 7.

Fig. 7. Toffoli Gate

2.3 Proposed Transistor Implementation Of Toffoli Gate

Fig. 7 shows the proposed transistor implementation of Toffoli Gate. In the proposed implementation, the outputs P and Q are directly generated from inputs A and B respectively by hardwiring. The proposed implementation is also suitable for both the forward as well as backward computation.

Forward Computation:

   P=A;   Q=B;

If A AND B =0 then R=C Else   R=C'

Backward Computation:

   A=P;   B=Q;

If P AND Q =0 then C=R Else

      C=R'

It takes 12 transistors for the proposed completely reversible implementation of the Toffoli gate, while   the existing implementation based on dual rail logic takes 16 transistors [6]. Thus, our proposed implementation achieves 25% reduction in terms of transistor count compared to existing one.
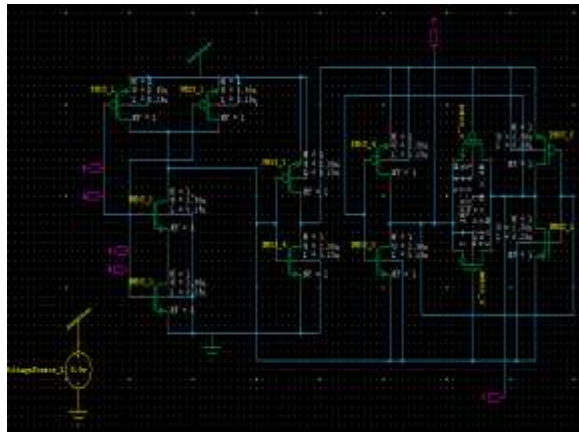
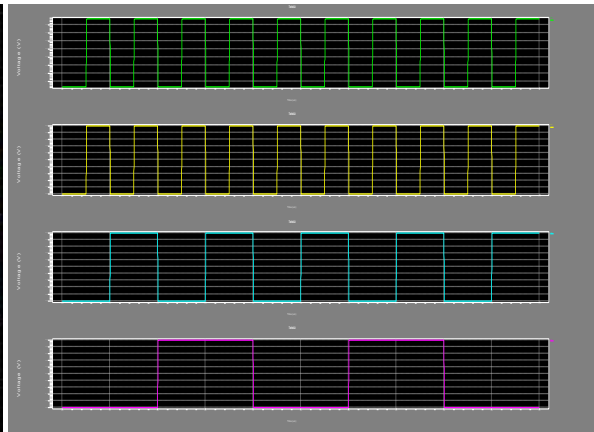**Fig. 8. Reversible Transistor Implementation Of The Toffoli Gate**

Fig. 9. Waveforms Of Reversible Transistor Implementation Of The Toffoli Gate

D. Peres Gate

Peres Gate (PG) [3, 4] is a 3*3 two- through reversible gate as shown in Fig. 10.
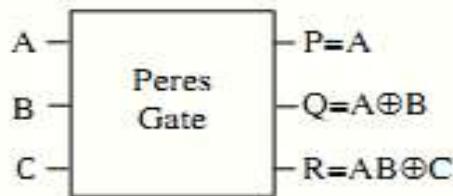

Fig.10. Peres Gate

2.5 Proposed Transistor Implementation Of Peres Gate

Fig. 10 shows the proposed transistor implementation of Peres Gate. In the proposed implementation, the outputs P is directly generated from input A by hardwiring. The proposed implementation is also suitable for both the forward as well as backward computation.
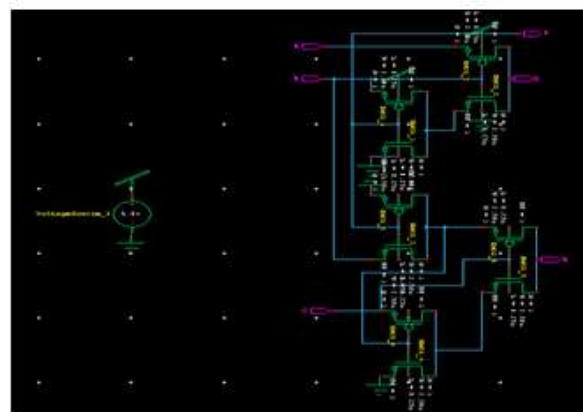

Fig. 11. Reversible Transistor Implementation Of The Peres Gate

After studding all above four reversible gate it is observed that, for partial product generation we have to choose any one out of these, according to their Minimum number of Gates required, Number of Constant inputs, and Minimum number of Garbage outputs.

Table-1 gives the comparative study of partial product generation of the circuit.

Table-1: Partial Product Generation

Reversible Gate	No. of Gates	No. of Constant Inputs	No. of Garbage Outputs
FG	40	40	32
FRG	40	40	32
TG	40	40	32
PG	28	40	32

The peres gate required less number of gates as compare to other reversible gates, hence we use the peres gate for partial product generation.

III. RELATED WORKS

The design of the multiplier is based on parallel operation .it is done using two steps.

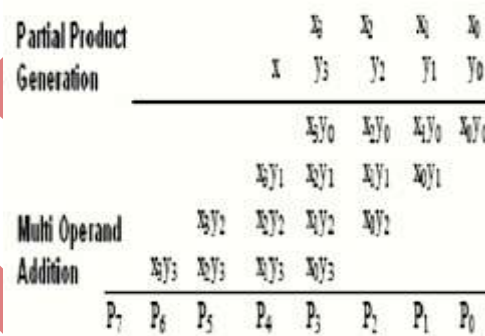Part i: Partial Product Generation (PPG)

Part ii: Summation Network

Fig. 12. Basic 4*4 Multiplication

As mentioned before, the purpose of this paper is the design of reversible fault tolerant multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The multiplier is implemented using PG and PFAG gates. The operation of a 4*4 reversible multiplier in Fig. 12. It consists of 16 Partial product bits of the four bit inputs X and Y to perform 4 * 4 multiplications.

3.1 Partial Product Generation (Ppg)

For partial product term generation the Peres gate is used. The Peres gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. Here by forcing the input C as logic 0 we get the product of inputs A and B in the output R. The P and Q are the garbage Outputs. Multiplier partial products are generated in parallel using 16 Peres gates shown in figure.

This uses 16 Peres gates for better circuit as it has less hardware complexity compared to other gates and moreover it posses parity preserving logic.
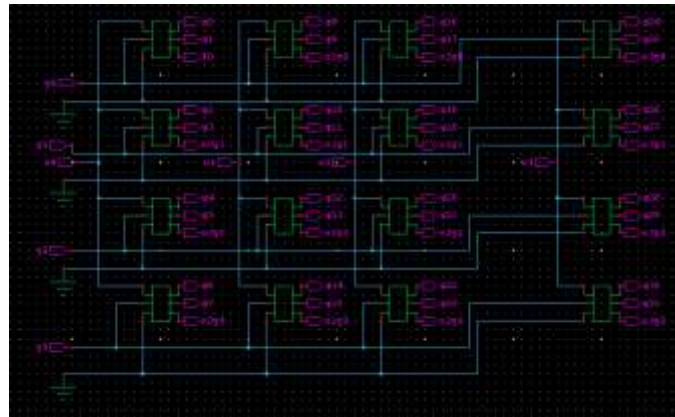

Fig.13. Partial Product Generation Using Peres Gate

3.2 Summation Network

The summation network needs TSG gate as a full adder (FA). Many reversible full adders have been proposed in the past. For example MKG and HNG gates can singly perform the full adder operation Design of multipliers with these gates indicates the different critical parameters for reversible multipliers. Experimental results of different reversible multiplier circuits in terms of speed, number of garbage outputs and constant inputs show the multiplier circuits with adders designed using IG gates have better results than multiplier circuits with MKG or HNG gates. The TSG gate shown in fig. 14 and its outputs shown in fig.15 which is used as full adder. It requires two constant inputs of logic 0 and produces the required sum and carry term with one garbage output. By forcing the input C as 0 it produces the sum and carry terms in outputs Q and R. Here P is the garbage output. It can also be further extended to implement full adder circuit which requires two constant inputs of logic 0 and two garbage values. The full adder implementation using TSG gate is shown in fig.16.
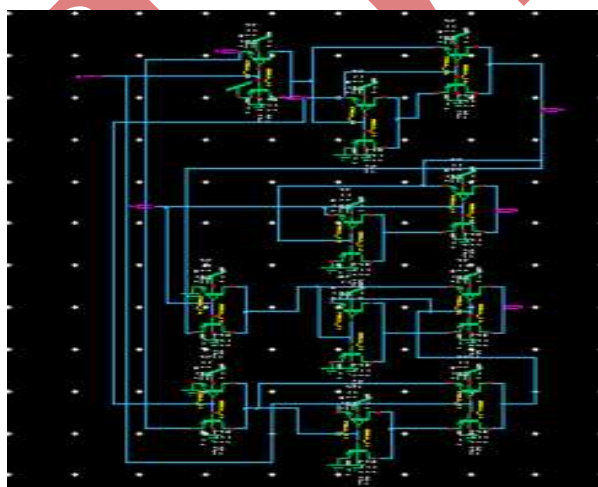

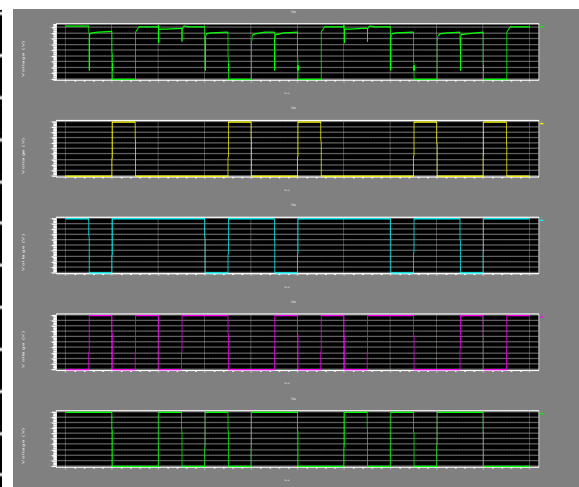**Fig.14. Reversible Transistor Implementation
Of The TSG Gate**

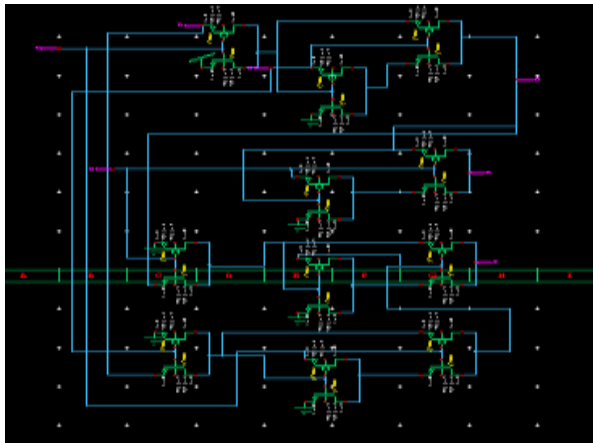**Fig. 15. Waveforms of Reversible Transistor
Implementation of TSG Gate**
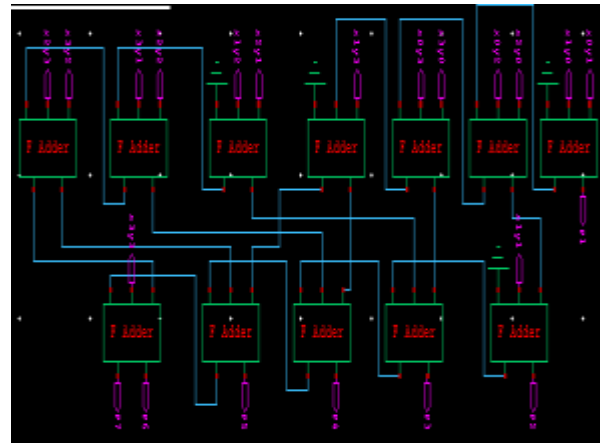
Fig. 16. Reversible Transistor Implementation   **Fig. 17. Proposed Summation Network using**
Of The TSG Gate As A Full Adder   **TSG Gate as a Full Adder**

The circuit of proposed summation network is shown in the fig. 17. It requires twelve TSG gate as full adder logic implementation. P_0 to P_7 is the product terms.

IV. OUR PROPOSED CIRCUIT

As mentioned before, the purposed of this paper is the design of reversible multiplier circuits with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The garbage outputs identified as the outputs which are not used in further computations and constants inputs need to realize only balanced functions.

This is the driving force that makes the proposal of new reversible multiplier circuit uses the modified full adder (MFA) [20] as shown in Fig. 18.
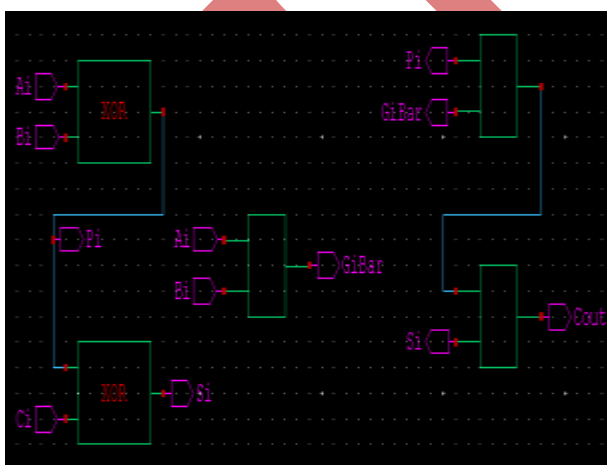
Fig. 18. MFA (Modified Full Adder)   **Fig. 19. Reversible Multiplier by using MFA**
                                                       (Modified Full Adder)
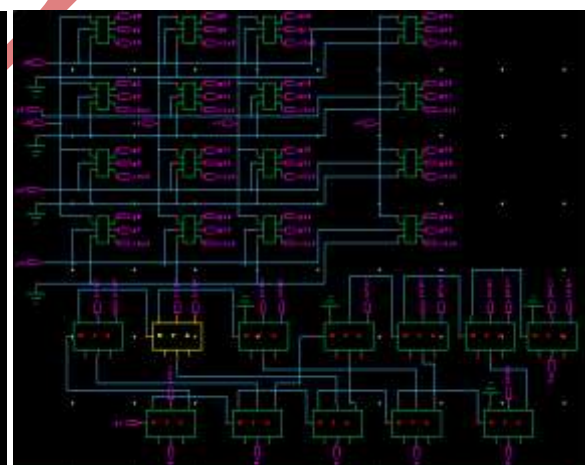
We propose the replacement of MFA by conventional reversible parallel adders of reversible multiplier circuit, were proposed in [21]. Further, the proposed full adder will be of great help in reducing the garbage outputs and constants inputs parameters. The reason for the fact that proposed reversible multiplier circuits use twelve modified full adders (MFA) that they produce zero garbage outputs and zero constants inputs.

V. RESULT AND DISCUSSION

The efficiency of proposed reversible multiplier depends on the choice of reversible gate. The efficient parallel adders will significantly improve the multiplier efficiency. The partial products can be generated in parallel using Peres gates and thereafter the addition is done of all product terms by using reversible parallel adder designed from TSG gates. After that we replace the reversible parallel adder by modified reversible adder then we compare both the multiplier and compare the terms like garbage outputs, power dissipation, number of gates required and number of constant inputs which shown in table 2.

Table-2: Comparison Of 4*4 Multiplier

Multiplier	Garbage Output	Constant Input	Number of Gates	Power Dissipation
Reversible Multiplier using TSG Gate	52	28	28	1.5 uW
Reversible Multiplier using MFA	40	28	28	0.9 uW

Thus, this paper provides the comparison of two multipliers according to their garbage outputs, power dissipation, number of gates required and number of constant inputs. The proposed multiplier is efficient in terms of number of Garbage outputs. The proposed 4*4 bit reversible multiplier is designed with minimum of 19 garbage outputs while the existing multiplier has 32 garbage outputs. Because of this garbage outputs the proposed multiplier will lead to a great reduction in power consumption. The simulation result for proposed multiplier is shown in Fig. 20 and the comparison table is also given in Table-3.

Table-3: Comparative Experimentalrusults Of Different Reversible Multiplier Circuits

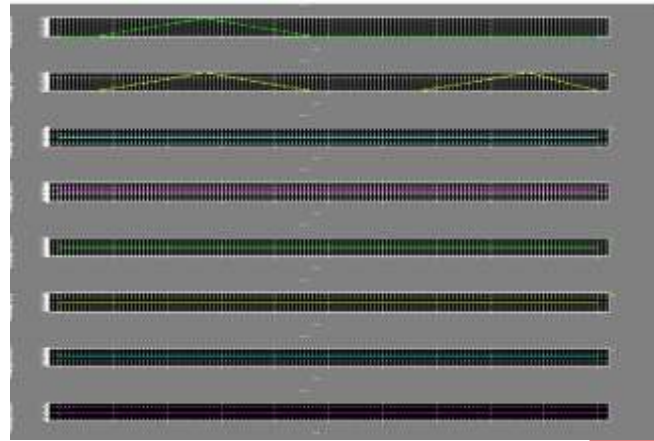| Reversible Multiplier	No. of Reversible Gate	No. of Constant Outputs	No. of Constant Inputs
Existing circuit with TSG	29	58	31
Existing circuit with MKG	28	56	29
Existing circuit with HNG	28	52	28
Our Proposed Design with MFA	28	36	20

Fig. 20. The simulation result for proposed multiplier (MFA)

VI.   CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic   units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. The focus of this paper is to reduce the number of garbage output. The reduction of garbage output reduces the power consumption. It is proved that the proposed multiplier (MFA) is better than the existing multiplier. In the proposed multiplier we synthesized a reversible multiplier circuit with the help of Peres gate. This circuit can be also helpful for high speed multiplier for dedicated hardware. The prospect for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

REFERENCE

[1]   R.Landuer, " Irreversibility and heat generation in the computing progress", IBM Journal of Research and Development, 5, pp.183-191, 1961.

[2]   C.H. Bennett "Logical Reversibility of Computation", IBM, J. Res. Develop, pp. 525-532, November 1973.

[3]   International Journal of Theor. Physics, 21(1982),pp.219-253.

[4]   T.Toffoli, "Reversible Computing",Tech memo MIT/LCS/TM-151,MIT Lab for Computer Science (1980).

[5]   W. C. Athas and L. J. Svensson, "Reversible Logic Issues in Adiabatic CMOS PhysComp, 1994, Proceedings, pages 111-118, IEEE. 1994.

[6]   Md. M. H Azad Khan,'Design of Full-adder with Reversible gates", International Conference on Computer and Information Technology, Dhaka, Bangladesh, 2002, pp.515-519.

[7]   M. Nielsen and I.Chuang, "Quantum   Computation   and   Quantum   Information",Cambridge University Press, New Delhi(2002).

[8]   A. De Vos ea al, "Design of Reversible Logic Circuits by means of Control Gates", PATMOS 2000, LNCS, 1918(2000) 255.

[9]   A. Desoete and A.De Vos, "A Reversible Carry-Look-ahead adder using Control Gates", Integration, VLSI J.,33(2002)88.

[10]   P. Kerntopf, "A New Heuristic Algorithm for Reversible Logic Synthesis", In Proceedings of the IEEE Design Automation Conference (2004) 834.

[11]   A. Agarwal and N. K. Jha, "Synthesis of Reversible Logic", Proceedings of IEEE, Design, Automation and Test in Europe Conference and Exhibitation, 2(2004) 1384.

[12]   D. M. Miller, D. Maslov, G. W. Duek, "A Transformation based algorithm for reversible logic synthesis", Proceedings of 40th Design Automation Conference(DAC'03), Anaheim, Califomia(2002) 318. [13] M. Mohammadi and M. Eshghi, On figures of merit in Reversible and Quantum Logic Designs, Quantum information Process, 8(2009) 297.

[13]   D. P. Vasudevan, "Reversible Logic Design with online Testability", IEEE Trans. Instru. And Meas., 55(2006) 406.

[14]   G.Schrom, "Ultra-Low-Power CMOS Technology", PhD, Technischen Universitat Wien (1998)

[15]   R. C. Merkle, "Two types of mechanical Reversible Logic. Nanotech, 4(1993)114.

[16]   E. Knill, R. La amme and G. J. Milbum, "A Scheme for Efficient Quantum computation with Linesr optics", Nature, 409(2001) 46.

[17]   H. Wood and D. Junghei Chen, "Fredkin gate circuits via recombination enzymes"Proceedings ceedings Evolutionary Computation 2004(CEC2004) 2(2004) 1896.

[18]   M. P. Frank, "Reversibility for Efficient computing" PhD. Dissertation, Dept. Elect. Eng. Comput. Sci., Mass. Inst. Tech., Cambridge, Jun. 1999.

[19]   H. Thaplyal and M. B. Srinivas, "Novel Reversible Multiplier Architecture using Reversible TSG gate" , IEEE Int. Conf Computer Systems and Applications (2006) 100

[20]   Yu-Ting Pai and Yu-Kumg Chen, "The Fastest Carry Look ahead Adder", Proceedings of the Second IEEE International Workshop on Electronic Design, Test and Applications (DELTA'04), 434-436.

[21]   M. Haghparast and K. Navi, " Design of a novel reversible multiplier circuit using HNG gate in nanotechnology", Am. J. Applied Sciences, 5 (2008)

[22]   Maryam Ehsanpour, Payman Moallem, Abbas Vafaei, "Design of a Novel Reversible Multiplier Circuit Using Modified Full Adder", 2010 International Conference on Computer Design And Applications (ICCDA 2010).

[23]   Himanshu Thapliyal and A. P. Vinod, "Transistor Realization of Reversible TSG Gate and reversible Adder Architectures" APCCAS 2006.

[24]   H. Thapliyal and M. B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate" Proc. IEEE International Conference on Computer Systems and Applications, PP. 100-103, March 2006.

[25]   Bui, Abdul Karim Al-Sheraidah, Yuke Wang, "New 4-Transistor XOR and XNOR", AP-ASIC, The second IEEE Asia Pacific Conference on ASIC, Aug 2000.

[26]   D. P. Vasudevan, P. K. Lala, J. P. Parkerson, "Reversible-Logic Design with online Testability", IEEE Transactions on Insrumentation and Measurements, VOL. 55, NO. 2, APRIL 2006, pp. 406-414.

[27]   Yingtao Jiang, Abdul Karim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer based low power Full Adder", IEEE Transactions on Circuits ans Systems-IEEE briefs, Vol 51, No 7, JULY 2004, pp 345-348.