INTEGRATED POWER ELECTRONIC MODULE

Hansa Gupta

EEE, Department, Kurukshetra University, (India)

ABSTRACT

***IPEM(Integrated Power Electronic Module) targets to develop a packaging technology which** provides three-dimensional planar packaging including a unique package resistance, better thermal transfer, lower parasitic problem and ultra-fast switching performance which is the major problem faced in creating a electronic circuit contains IGBT, MOSFET , SOD etc (Power electronic devices) . It also meets the increased requirements towards ampacity and heat dissipation, Increasing power levels and power density for multiple end products, not only in new but also in already established packages. It overcome the given package limitations and provides an easy way to cool the devices and to connect them to the outer circuit. It provides a very compact and efficient way to design an electronic circuit.*

Keyword: IPEM, IGBT, MOSFET, DCB, PCB

I. INTRODUCTION

The fundamental approach to power conversion has steadily moved toward high-frequency synthesis resulting in important reductions in converter performance, size, weight and cost. However, in some high frequency power conversion technologies ,fundamental limits are being reached that will not be overcome without a radical change in the design and implementation of power electronics systems. It is well recognized within the industrial sector that the performance of power electronics systems were driven by improvements in semiconductor components over the last decades. Moving from bipolar to MOSFET technology has resulted in speed increases that, today, test the limits of packaging inductance and thermal handling. Thus, an order of magnitude increase in switching speed, which is possible with new device technologies, will require substantial reductions in structural capacitances and inductances associated with device and system-level packaging. For a typical power electronics system, individual power devices are mounted on the heat sink, and the drivers, sensors, and protection circuits are implemented on a printed circuit board and mounted near the power devices. The manufacturing process for such equipment is labour and cost-intensive. However, some manufacturers have taken a more aggressive approach in recent years, developing a high level of integration where power semiconductors in the die form are mounted on a common substrate with wire bonding. Although the wire bonding technology has seen many improvements in reliability, this approach still limits the possibilities of three-dimensional integration, as well as having electromagnetic layout constraints. The thermal management in this type of packaging is essentially limited to one-dimensional heat flow, while the reduction of structural inductance associated with bonding wires have limitations. It is perceived, how however, that power electronics modules constitute one of the driving forces towards modularization and integration of power electronics systems. Recent innovations in power modules have been mostly pushed by semiconductor development with the help of improved layout and packaging technologies. The development trends are focused on increasing current and voltage levels, increasing temperature, enhancing reliability and functionality, as well as reducing size, weight and cost New ideas on power modules include the reduction of the number of interfaces to reduce the number of solder layers and the risk of solder imperfections and thermal fatigue. Another concept that has been around is the elimination of the base plate from the power module, first observed at low power and now migrating to higher power applications. In terms of reliability improvement, devices using low temperature joint (LTJ) technology do not change their thermal resistance after extensive power cycles (>50 000), as opposed to devices using low temperature conventional solder techniques that achieve the end of useful life after 30 000 power cycles While semiconductor devices are still one of the dominant barriers for future power system development, devices do not currently pose the fundamental limitation to power conversion technology. It is rather packaging, control, thermal management, and system integration issues that are the dominant technology barriers currently limiting the rapid growth of power conversion applications. To address some of these issues, this paper briefly discusses the technology advancements needed to improve the characteristics of power electronics systems, as well as the technologies being developed for integration of multi-kilowatt power electronic equipment. Among these technologies being developed are the planar metalization device interconnect, that allows three-dimensional integration of power devices, and the integration of power passives to increase the power density, mainly for power supply applications. The technologies being developed span a wide range of applications from distributed power systems to motor drives. The development of packaging techniques, integration of current sensors and the development of power semiconductor devices to either improve performance or to facilitate integration of power electronics systems are addressed hereafter.

This paper also discusses results obtained from the various technologies being developed within the research scope of the Centre for Power Electronics Systems (CPES), whose mission is to promote an integrated approach to power electronics systems in the form of highly Integrated Power Electronics Modules (IPEMs).

II. MAIN CONSTITUENTS OF POWER MODULE

- DCB for electrical isolation
- Power Semiconductors
- Bond Wires provide internal links
- Phase change material

2.1 Dcb For Electrical Isolation

DCB (Direct Copper Bonded) sometimes also named as DBC (Direct Bonded Copper) technology denotes a special process in which the copper foil and the Al2O3 or AIN (one or both sides) are directly bonded under appropriate high temperature. The super-thin DCB substrate has excellent electrical isolation, high thermal conductivity, fine solderability and high bonding strength. It can be etched like normal FR4 PCB, but has a high current loading capability. Therefore DCB ceramic PCB has become the base materials of construction and interconnection technology of high power semiconductor telectronic circuits and also have been the basis for the "Chip On Board" (COB) technology which represent the packaging trend in the future.

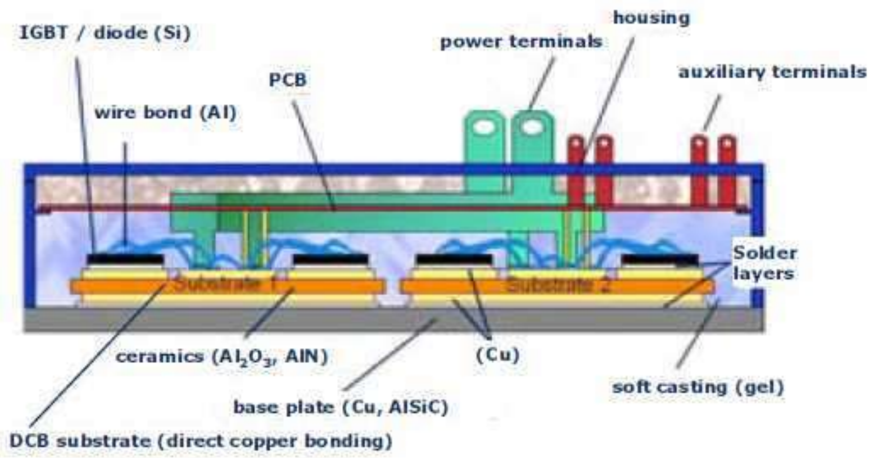

Fig2.1 Crossectional View Of IPEM Showing DCB Substrate

2.1.1 Characteristics Of Dcb Ceramic PCB –

- High mechanical strength, mechanically stable shapes. Hight strength, fine thermal conductivity, excellent electrical isolation. Good adhesion, corrosion resistant;
- Excellent thermal cycling capabilities (up to 50,000 cycles), high reliability;
- Can be etched to various layout like normal FR4 PCB;
- No contamination, free of environmental problem;

2.1.2 DCB Ceramic PCB Design Guide

Because its special characteristics of DCB ceramic board, you cannot design DCB PCB following normal FR4 PCB design rule. Here are simple design guide for DCB ceramic printed circuit board.

- Conductor material: Copper, thickness 0.1mm ~0.3mm.
- Copper thickness VS trace space & trace width For 0.1mm (3OZ) copper thickness, trace space & width should be 0.3mm 0.2mm copper, 0.4mm space & width; 0.3mm copper, 0.5mm space & width.
- Maximum effective working area: 126x176mm
- Substrate (Al2O3 & AIN) thickness: 0.25mm (seldom used, extreme expensive), 0.38mm, 0.50mm, 0.63mm(standard), 0.76mm, 1.0mm, and 1.27mm (only for AIN)
- There should be 0.3mm margin between trace and edge of board at each side for 0.1mm thickness copper; 0.4mm margin for 0.2mm copper thickness; 0.5mm margin for 0.3mm copper thickness;
- Surface finishing: Nickel (1~7um); or Aug plating (0.075~0.1um, 3-4 u")
- No solder mask is better (working tempature is -55~+850C, as most of ceramic board was working in high temperature > 200C, no good oil is suitable for that temperature range)
- We will ship via single piece, as Al2O3 need to be cut by laser and not easy de-panel like normal FR4 PCB
- ore hole, more expensive. Min hole: 0.15mm, no Max. Hole diameter > 0.5mm will be better in price.
- Normally trace should be related much simple compared with FR4 board

Wide application temperature: -55C~850C. The thermal expansion coefficient is closed to that of silicon, simplify the production technology of power module

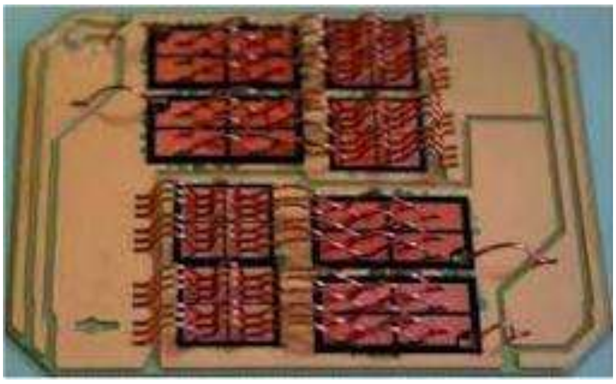

Fig.2.2 DCB Substrate with 400µm Cu Wire Bonds On Cu Metalised IGBTS

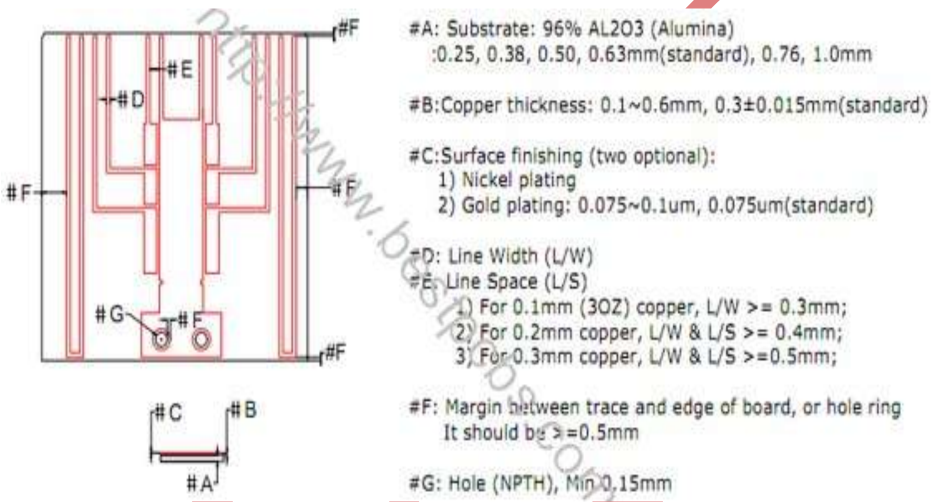

Fig.3 DCB Ceramic PCB Design Rule Picture

2.2 Power Semiconductors

A power semiconductor device is a semiconductor device used as a switch or rectifier in power electronics; a switch-mode power supply is an example. Such a device is also called a power device or, when used in an integrated circuit, a power IC. Intelligent digital power ICs came up in the last decade. A power semiconductor device is usually used in "commutation mode" (i.e., it is either on or off), and therefore has a design optimized for such usage; it should usually not be used in linear operation.

2.2.1 Some Common Devices

Some common power devices are- Power diode, thyristor, power MOSFET, and IGBT. The power diode and power MOSFET operate on similar principles to their low-power counterparts, but are able to carry a larger amount of current and are typically able to support a larger reverse-bias voltage in the off-state. Structural changes are often made in a power device in order to accommodate the higher current density, higher power dissipation, and/or higher reverse breakdown voltage. The vast majority of the discrete (i.e., non-integrated) power devices are built using a vertical structure, whereas small-signal devices employ a lateral structure. With the vertical structure, the current rating of the device is proportional to its area, and the voltage blocking capability is achieved in the height of the die. With this structure, one of the connections of the device is located on the bottom of the semiconductor die.

2.2.2 Chart

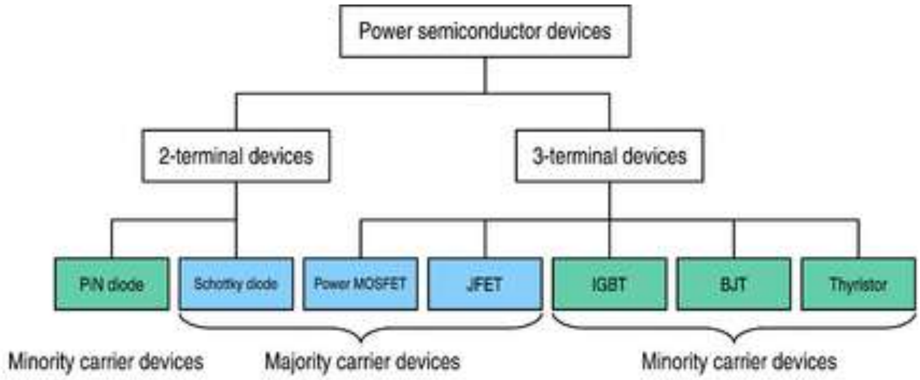

Fig.2.3 Classification Of Power Semiconductors

2.3 Bond Wires Provide Internal Links

Wire bonding is the method of making interconnections between an integrated circuit (IC) or other semiconductor device and its packaging during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another. Wire bonding is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.

Bondwires usually consist of one of the following materials:

- Aluminum
- Copper
- Silver
- Gold

The main classes of wire bonding:

- Ball bonding
- Wedge bonding
- Compliant bonding

2.3.1Ball Bonding

Ball bonding is a type of wire bonding, and is the most common way to make the electrical interconnections between a chip and the outside world as part of semiconductor device fabrication. Gold or copper wire can be used, though gold is more common because its oxide is not as problematic in making a weld. If copper wire is used, nitrogen must be used as a cover gas to prevent the copper oxides from forming during the wire bonding process. Copper is also harder than gold, which makes damage to the surface of the chip more likely. However copper is cheaper than gold and has superior electrical properties, and so remains a compelling choice. Almost all modern ball bonding processes use a combination of heat, pressure, and ultrasonic energy to make a weld at each end of the wire. The wire used can be as small as 15 μm in diameter — such that several welds could fit across the width of a human hair. A person upon first seeing a ball bonder will usually compare its operation to that of a sewing machine. In fact there is a needle-like disposable tool called the *capillary*, through which the wire is fed. A high-voltage electric charge is applied to the wire. This melts the wire at the tip of the capillary. The tip of the wire forms into a ball because of the surface tension of the molten metal. The ball quickly solidifies, and the capillary is lowered to the surface of the chip, which is typically heated to at least 125°C. The machine then pushes down on the capillary and applies ultrasonic energy with an attached transducer. The combined heat, pressure, and ultrasonic energy create a weld between the copper or gold ball and the surface of the chip - which is usually copper or aluminum. This is the so-called *ball bond* that gives the process its name. (All-aluminum systems in semiconductor fabrication eliminate the "purple plague"—a brittle gold-aluminum intermetallic compound—sometimes associated with pure gold bonding wire. This property makes aluminum ideal for ultrasonic bonding.) Next the wire is passed out through the capillary and the machine moves over a few millimeters to the location that the chip needs to be wired up to (usually called theleadframe). The machine again descends to the surface, this time without making a ball so that the wire is crushed between the leadframe and the tip of the capillary. This time the surface is usually gold, palladium, or silver - but the weld is made in the same way. The resulting weld is quite different in appearance from the ball bond, and is referred to as the wedge bond, tail bond, or simply as the second bond. In the final step the machine pays out a small length of wire and tears the wire from the surface using a set of clamps. This leaves a small tail of wire hanging from the end of the capillary. The cycle then starts again with the high-voltage electric charge being applied to this tail.

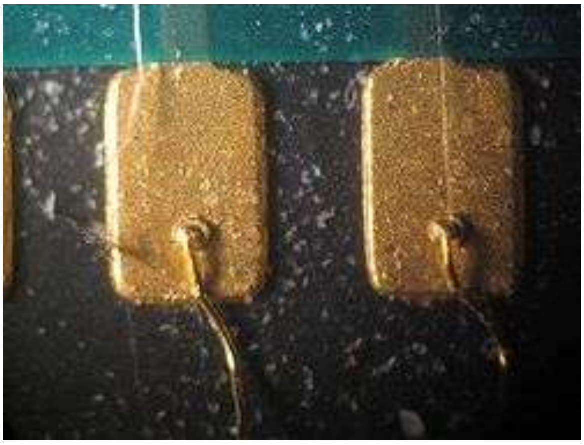

Fig2.4 Showing Ball Bonding Using Gold

3.2 Wedge Bonding

Wedge-wedge wire bonding is the oldest semiconductor assembly process dependent solely on acoustic energy. There are a few exceptions where thermal energy (heat) is combined to further improve the welding action. The dominant ultrasonic frequency has been for many years 60kHz. It is even lower on some applications where larger diameter wire (>38µm) is used. This was until the early 1990’s when Japanese researchers, following the development and publications of Texas-based researchers, learned about the process improvements when higher ultrasonic frequencies (>60kHz) are used to bond gold wire to aluminum bond pads. Their investigation confirmed the improvements in weld reactivity (less open bond) and faster bond cycles. The major discovery was the fact that welding begins as soon as the wire contacts the surface to be bonded, creating a new welding pattern characterized by a series of parallel welding lines. The new welding pattern does not follow the traditional low frequency pattern where the center of the bond is voidedand surrounded by a welded ring. It has been published that during the welding process, lower ultrasonic frequencies begin utilizing some of the energy on wire deformation,followed by the actual welding process therefore the voided center.

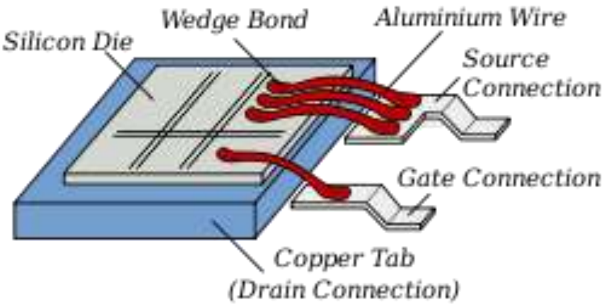

Fig.2.5 Showing Wedge Type Wire Bonding

2.3.2 Compliant Bonding

Compliant bonding is used to permanently connect fine gold wires to various critical components such as the silicon integrated circuit or "Chip" which is the "brains" in most microelectronic packages. It was first introduced by Alexander Coucoulas in the 1960's. The bond is formed well below the melting point of the mating gold surfaces and is therefore referred to as a solid-state type bond. The Compliant bond is uniquely formed by transmitting heat and pressure to the bond region through a relatively thick indentable or "compliant medium" which is generally used in the form of an aluminum tape. The two forms of integrated circuits discussed above were the beam leaded integrated circuit composed of attached electroformed gold leads or beams and the silicon integrated circuit chip. With respect to the Beam leaded silicon chip, both Compliant and Thermocompression Bonding can be employed since each have their advantages. At this time, the most widely used form is the silicon integrated circuit chip, without the beam leads, which therefore requires electrical connections directly to the metallized silicon Chip. If wire connections is the method of choice to form these connections, Thermosonic bonding gold wires directly to the silicon chip has been the process most widely used because of its proven reliability as a result of the low bonding parameters of force, temperature and time needed to form the bond.

2.4 Phase-Change Material (Pcm)

A phase-change material (PCM) is a substance with a high heat of fusion which, melting and solidifying at a certain temperature, is capable of storing and releasing large amounts of energy. Heat is absorbed or released when the material changes from solid to liquid and vice versa; thus, PCMs are classified as latent heat storage (LHS) units.

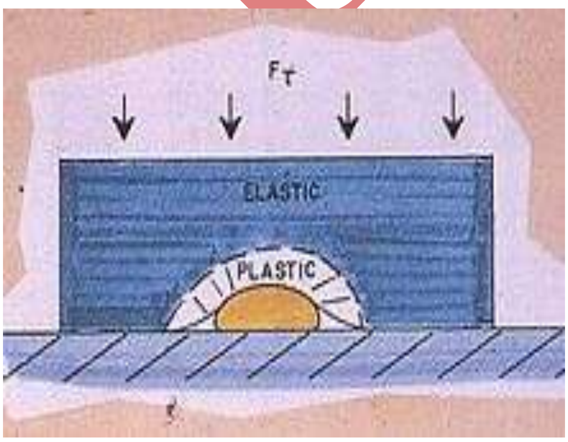

Fig 2.6 Internal Bonding Of Compliant Bonding

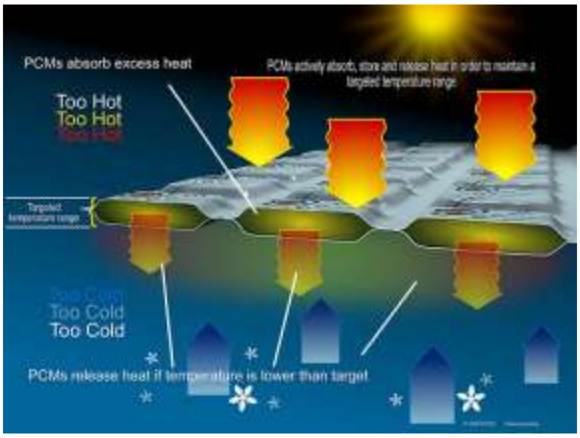

Fig2.7 Showing Working Of PCM

2.4.1 Characteristics And Classification Of PCM

PCMs latent heat storage can be achieved through solid–solid, solid–liquid, solid–gas and liquid–gas phase change. However, the only phase change used for PCMs is the solid–liquid change. Liquid-gas phase changes are not practical for use as thermal storage due to the large volumes or high pressures required to store the materials when in their gas phase. Liquid–gas transitions do have a higher heat of transformation than solid–liquid transitions. Solid–solid phase changes are typically very slow and have a rather low heat of transformation. Initially, the solid–liquid PCMs behave like sensible heat storage (SHS) materials; their temperature rises as they absorb heat. Unlike conventional SHS, however, when PCMs reach the temperature at which they change phase (their melting temperature) they absorb large amounts of heat at an almost constant temperature. The PCM continues to absorb heat without a significant rise in temperature until all the material is transformed to the liquid phase. When the ambient temperature around a liquid material falls, the PCM solidifies, releasing its stored latent heat. A large number of PCMs are available in any required temperature range from −5 up to 190 °C.[1] Within the human comfort range between 20–30 °C, some PCMs are very effective. They store 5 to 14 times more heat per unit volume than conventional storage materials such as water, masonry or rock.

III. RESULT

Figure shows the simulated waveform of drain source voltage. With active IPEM, the voltage overshoot is reduced to 416V compared with 460V for discrete version. The turnoff loss is reduced from 48uJ to 25uJ by using IPEM. Considering 200kHz operation of DC/DC converter, the turn-off loss is reduced by 8W with 4ohm gate resistance. This translated into about 1% efficiency increase of the front-end converter and 10% loss Figure 11 and Figure 12 shows the improvements of active IPEM for different gate resistance. With passive IPEM, all the passive components except output filter capacitor are integrated into one single package. This could greatly reduce the volume of passive components They are shown in Figure13,14,15. All three prototypes are asymmetrical half bridge with current doubler. First prottype is based on discrete passive design. Second prototype use integrated magnetic technology. Third prototype is built with passive and active IPEM. With discrete passive components, the total volume of passive components is 343cm3. By applying integrated magnetic concept, it is reduced to 258cm3. With passive IPEM, all the passive components except output filter capacitors are integrated. A volume of 87cm3 is achieved, which is five times improvement as shown in Table 3-1

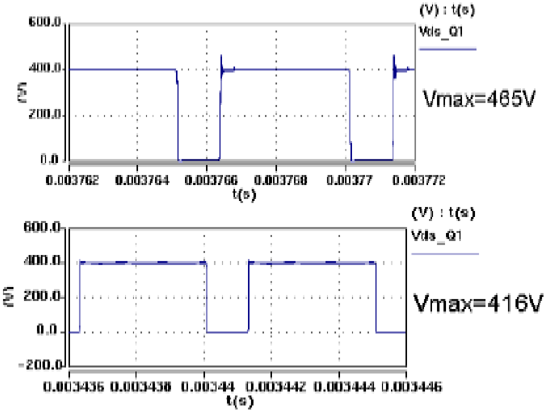

Fig 3.1 Simulation Waveform of (a) Discrete(b)IPEM

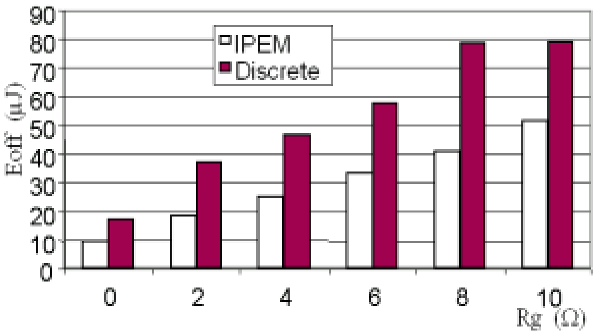

Fig3.2 Active IPEM Turn-Off Loss Reduction

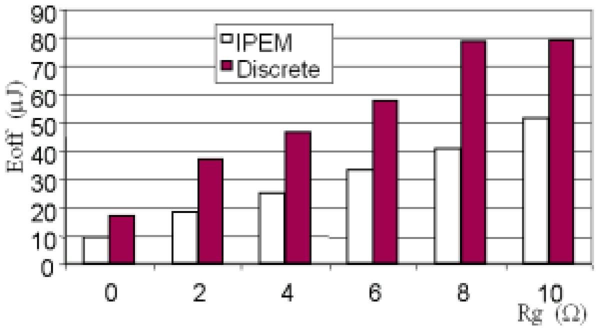

Fig3.3 Voltage Overshoots Improvement By IPEM

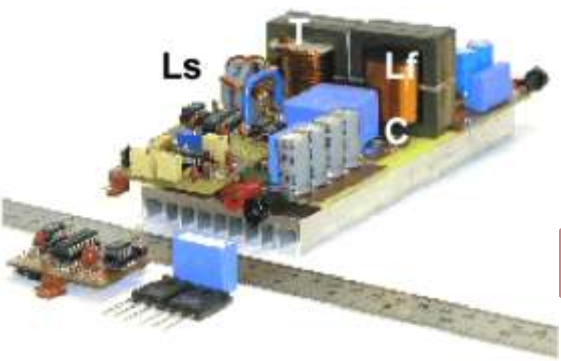

Fig3.4 Discrete Design

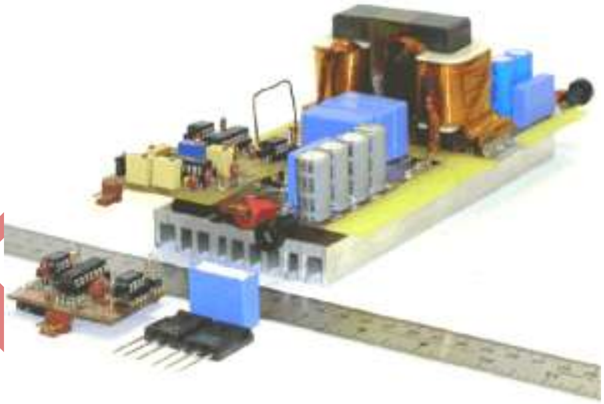

Fig3.5 Integrated Magnetic Design

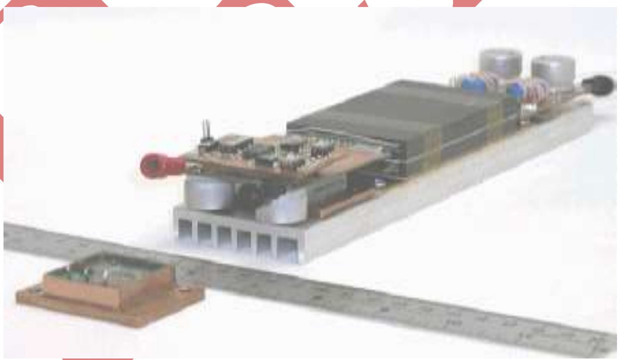

Fig3.6 IPEM

Parameters	*Prototype 1*	*Prototype 2*	*Prototype 3*
No. of passive components	6	4	1
Volume of passive components (cm^3)	173	151	82
No. of terminals	15	12	5
Volume of terminals (cm^3)	170	107	5
Total passive volume (cm^3)	343	258	87
System Profile	2U	2U	1U
System Power Density	1	X1.2	X3.6

Fig 3.7 Table 3-1Comparison Of Above Three Prototypes

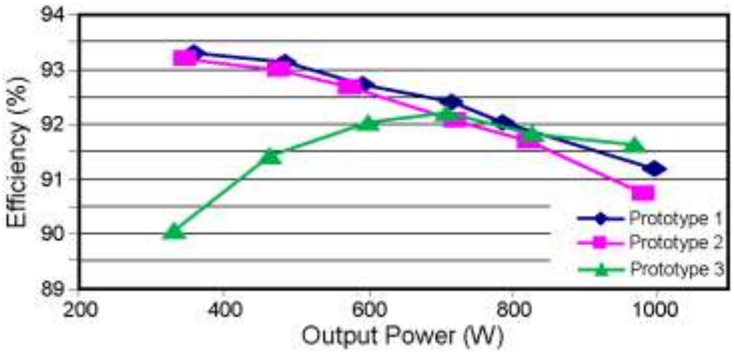

Fig3.8 Test Efficiency Of Three Prototypes

IV. CONCLUSION

It has been proved as a very important tool for circuit designers. It is beneficial in many ways as it :

- Provides short communication path
- It mnimises Stray Inductance.
- Improves Switching Behaviour
- Lmits transient overvoltages.
- Provides better thermal resistance
- Compact in size

Above all above written properties. It saves time to construct a circuit which contains the power electronics equipments and minimises the space occupied by the Power circuit .

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