NOVEL OSCILLATORS IN SUBTHRESHOLD REGIME

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ABSTRACT

In this paper, the implementation of oscillators in the subthreshold region is proposed. The ring and coupled ring oscillators are implemented. The techniques of swapped body biasing (SBB) and Dynamic threshold Voltage MOSFET (DTMOS) biasing are introduced for performance improvement of coupled ring oscillators. The functionality of the oscillators in subthreshold region is verified through simulations using 180 nm CMOS technology parameters. A comparison in performance of the oscillators is carried out. It is found that coupled ring oscillator based on the two biasing techniques shows improved performance.

Keywords: Coupled Ring Oscillator, Dynamic Threshold Voltage MOS Biasing, Ring Oscillator, Subthreshold Region, Swapped Body Biasing.

I. INTRODUCTION

The development of the applications demanding low energy application has generated significant scope for subthreshold circuits [1-5]. These circuits are suitable for two type of portable devices. There are energy constraint systems at one hand where the aim is energy conservation and speed of operation is largely irrelevant. The other application need high performance for fraction of time they are operational and spend significant time in non-critical tasks. The mobile phone is apparent example of the later class as it often remains in near idle computation mode while waiting for input from wireless link or user. Oscillator is a key component in a phase-locked loop (PLL) for providing the timing basis in clock control, data recovery, and synchronization [6]. It is also an integral part of voltage controlled oscillator which is employed in a wide variety of applications such as disk-drive read channels, on-chip clock distribution, integrated frequency synthesizers and microprocessor clock generation [7]. This paper proposes the implementation of two ring oscillators in subthreshold region. The first implementation uses a chain of odd numbers of CMOS inverters operating in subthreshold region. In the second implementation, a coupled ring oscillator [6] capable of producing quadrature outputs is proposed. The paper first briefly presents the operation of a MOSFET in subthreshold region in section II. The implementations of the ring and coupled ring oscillators in subthreshold region are presented in the section III. The different biasing techniques used for implementation are described briefly in section IV. The simulation results are presented in section V using CMOS 180nm technology parameters. The conclusion drawn from the results appear in section VI.

II. SUBTHRESHOLD DIGITAL DESIGN

The surface of the Metal-Oxide Semiconductor (MOS) structure is weakly inverted when the gate voltage is sufficient to cause band bending at the surface ranges between φF and 2φF. This region is also called subthreshold and current flows when drain to source potential is applied. The current flow mechanism is similar to that in bipolar transistors i.e. drain current shows exponential dependence on gate to source voltage. This current is called subthreshold current and is primarily a leakage current which flows even when gate to source voltage is below threshold voltage.

In the subthreshold, the power supply voltage VDD is made less than its threshold voltage V_{th}. In this case, the drain current I_{ds} region is exponentially related to the gate voltage V_{gs} as shown in Equation (1) [3]:

$$I_{sub} = I_0 \exp\left(\frac{V_{gs} - V_T}{nV_{th}}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_{th}}\right)\right) \quad (1)$$

where V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source voltage, n is the subthreshold slope factor and V_{th} is temperature equivalent of voltage (V_{th} = kT/q, where k is the Boltzmann constant, T the absolute temperature, and q the electron charge. The factor n of a long-channel uniformly doped device is calculated as:

$$n = 1 + \frac{C_b}{C_g} \quad (2)$$

where C_g and C_b are the gate and bulk capacitances respectively.

A MOSFET operating in subthreshold region offers several advantages. The MOSFETs operating in this region generate low levels of the drain current, thereby creates a high-value resistor. These MOSFETs show low dynamic power consumption due to the lowering of power supply and the drain current [5]. Based on these advantages, we propose the implementation of ring oscillators in the subthreshold region.

III. RING OSCILLATOR

A ring oscillator (RO) is one of the most commonly used components in many integrated systems. The unique features of RO include ease of design with the state-of-art integrated circuit technology (CMOS, BiCMOS), ability to oscillate at lower values of voltage, high frequency oscillations can be achieved, electrically tunable with wide tuning range; attainment of multiphase outputs. Two popular implementations of a ring oscillator have been used in this paper. An RO is a cascade of odd number of delay stages connected in a close loop chain. Fig. 1 shows the traditional CMOS inverter and a ring oscillator using seven inverters. The frequency of oscillation of an RO varies with propagation delay τd of the individual inverter stage and the number of inverter stages used in the ring structure. There must be a phase shift of 2π and unity voltage gain at the oscillation frequency to achieve self-sustained oscillation. In a RO with m inverter stages, a phase shift of π/m is provided by each stage while the remaining phase shift of π is provided by the dc inversion. The signal undergoes m delay

stages in a time of $m\tau d$ to provide a phase shift of π and for another time in a time period of $2m\tau d$ to obtain the remaining phase of π [8]. Therefore, the frequency of oscillation *fo* can be found out using (3):

$$f_o = \frac{1}{2m\tau d} \quad (3)$$

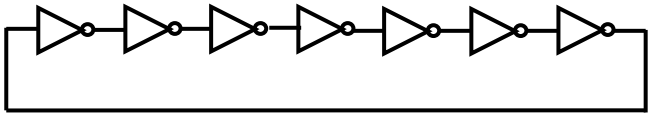

Fig. 1. Ring Oscillator with 7 inverter stages

A coupled ring oscillator (CRO) is designed by coupling two ring oscillators in such a way that only four distinguished nodes are formed. These four nodes generate quadrature outputs having a phase difference of 900 for a completely symmetrical coupling [6]. The implementation of a coupled ring oscillator employing 8 inverter stages is shown in Fig. 2.

IV. BODY BIASING TECHNIQUES

A CMOS inverter operating in the subthreshold region suffers from a drawback of reduced switching speed. This can be addressed by adopting body biasing techniques such as the swapped body biasing (SBB) [9] and the dynamic threshold MOS (DTMOS) biasing technique [10]. In SBB technique, the substrate of the NMOS devices are tied to the power supply voltage V_{DD} whereas those of the PMOS devices are tied to ground. Swapping the bulk terminals of the two MOSFETs increases the drive currents in the subthreshold operation from an exponential current increase, but degrades output node voltages when V_{DD} is greater than the zero bias threshold voltage [5]. Thus, SBB technique provides improved performance under subthreshold supply voltages. A CMOS inverter implemented using SBB technique is shown in Fig. 3. In DTMOS biasing technique, the substrate of the transistor is tied to its gate to allow the threshold voltage to change dynamically with the gate input voltage. With the increase in the gate voltage, the threshold voltage drops resulting in a much higher current drive than standard MOSFET for low-power supply voltages. A CMOS inverter implemented using DTMOS biasing technique is shown in Fig. 4. In this paper, the coupled ring oscillator (Fig. 2) is implemented using inverters with traditional biasing (Fig. 1), SBB (Fig. 3) and DTMOS biasing (Fig. 4).

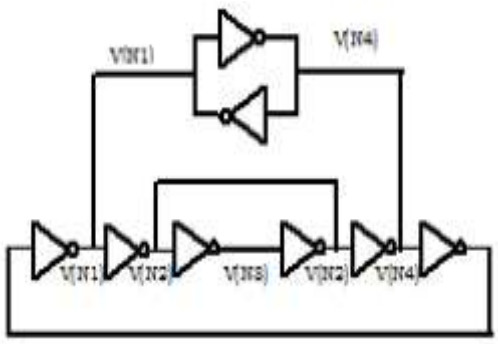

Fig. 2. Coupled Ring Oscillator Two Coupled 3-Stage Ring Oscillator

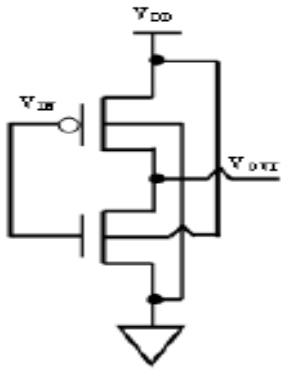

Fig.3. A CMOS Inverter Based On Swapped Body Biasing Technique

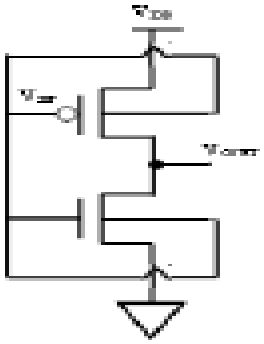

Fig. 4. A CMOS Inverter Based On DTMOS Biasing Technique

V. SIMULATION RESULTS

In the first sub-section, the functionality of ring oscillators in subthreshold region (Fig. 1) is verified. Further, the CRO is implemented using the inverters based on traditional, SBB and DTMOS biasing techniques. Then in the second section, the results of the comparison in performance of the ring oscillator and coupled ring oscillator are presented. All the simulations are carried with SPICE using 180 nm CMOS technology parameters. A power supply and load capacitor of 0.37 V and 1 fF have been taken in simulations respectively.

a. Functional Verification

The ring oscillator (Fig. 1) and the coupled ring oscillator (Fig. 2) are simulated. The waveform obtained for the ring oscillator output is shown in Fig. 5. It can be observed that the ring oscillator conforms to the functionality. The waveforms obtained at the four output nodes of the coupled ring oscillator using DTMOS biasing technique is shown Fig. 6. The waveforms for the coupled ring oscillator using traditional and SBB biasing are not shown for the sake of brevity

b. Performance Comparison

The simulation results for the ring oscillator and the coupled ring oscillator are listed in Table I. The results show that the coupled ring oscillators using SBB and DTMOS biasing techniques are better than the ring oscillators. It can be observed that the frequency of oscillation of the coupled ring oscillators increases by 16.62 MHz, 18.09 MHz in SBB and DTMOS biasing techniques respectively, with respect to traditional biasing. Though the power consumption increases by 859 nW and 757 nW respectively for both the techniques. Also, the SBB and DTMOS biasing based coupled ring oscillator outperforms the ring oscillator by reducing the propagation delay by 76.82 ns and 78.17 ns respectively.

TABLE I. PERFORMANCE COMPARISION OF OSCILLATORS

Performance Parameters	Ring Oscillator	Coupled Ring Oscillator		
		Traditional Biasing	Swapped Body Biasing	DTMOS Biasing
Frequency of oscillation (MHz)	2.19	2.954	19.571	21.040
Propagation Delay (ns)	50.53	89.822	13.008	11.654
Power Dissipation (W)	5.6×10^{-8}	1.14×10^{-7}	9.73×10^{-7}	8.71×10^{-7}

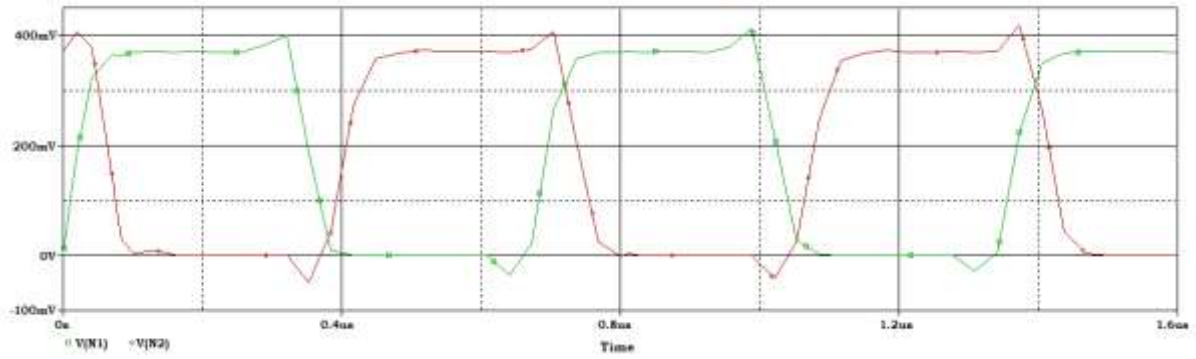

Fig. 5. Output Waveform Of Ring Oscillator Using Traditional Biasing

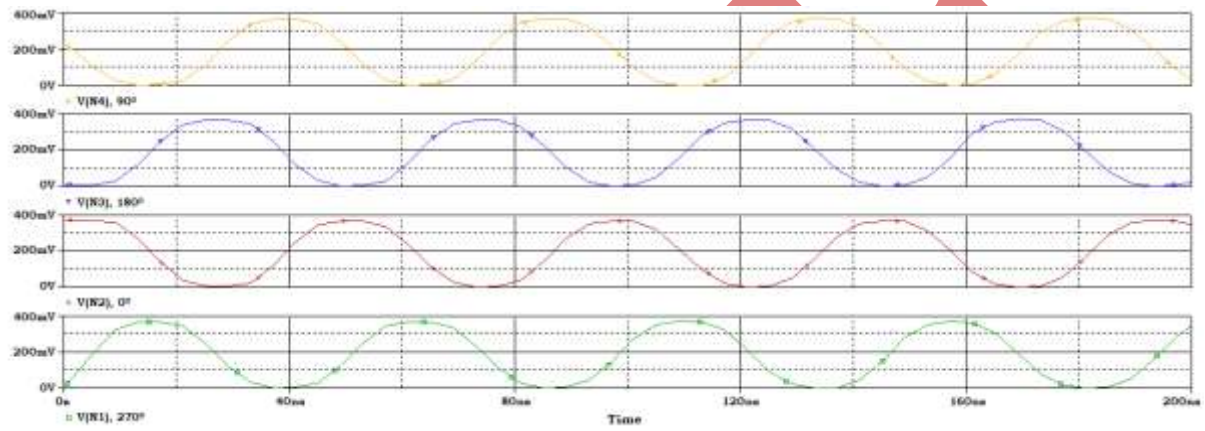

Fig. 6. Output Waveform Of Coupled Ring Oscillator Using DTMOS Biasing Technique

VI. CONCLUSION

This paper proposes the implementation of oscillators in the subthreshold regime. The ring and coupled ring oscillators are implemented. Improved CRO implementations based on swapped body biasing technique and dynamic threshold MOS biasing technique are proposed. The feasibility of the oscillators in subthreshold region is studied through simulations using 180 nm CMOS technology parameters. A comparison in performance of the oscillators show that the coupled ring oscillators based biasing techniques improves the performance significantly.

REFERENCES

[1] M. Alioto, "Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis", IEEE Transactions on Circuits and Systems-I, Vol. 57, No. 7, July 2010, 1597-1607.

[2] H. Soeleman and K. Roy, "Digital CMOS Logic Operation in the Sub Threshold Region" CM Great Lakes Symposium on VLSI 2000: 107-112.

[3] A. Wang, B. H. Calhoun, A. P. Chandrakasan, "Sub-threshold Design for Ultra Low-Power Systems", Springer, 2006.

[4] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," IEEE J. Solid-State Circuits, vol. 40, no. 1, Jan. 2005, 310-319.

[5] J. Rabaey, J. Ammer, B. Otis, F. Burghardt, Y. H. Chee, N. Pletcher, M. Sheets, and H. Qin, "Ultra-low-power design—The Roadmap to disappearing electronics and ambient intelligence," IEEE Circuits Devices Mag., pp. 23–29, Jul./Aug. 2006.

[6] J. Baker, H. W. Li, D. E. Boyce, "CMOS, Circuit Design, Layout, and Simulation", Wiley, 1997.

[7] I. A. Young, J. K. Gearson and K. L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessor," IEEE Journal of Solid State Circuits, Vol, 27, No. 11 1992. 51-52

[8] M.K. Mandal and B.C. Sarkar, "Ring Oscillators: Characteristics and applications", Indian Journal of Pure & Applied Physics Vol. 48, February 2010, 136-145.

[9] J. Nyathi, B. Bero and R. McKinlay, "A Tunable Body Biasing Scheme for Ultra-Low Power and High Speed CMOS Designs," International Symposium on Low Power Electronics and Design - 2006. October 4-6, 2006.

[10] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, vol. 44, No. 3, March 1997. 414-422.