# MODELING OF 5-LEVEL CHB AS DSTATCOM FOR COMPENSATION OF POWER QUALITY ISSUES

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***ABSTRACT***

*With the widespread use of harmonic generating devices, the control of harmonic currents to maintain a high level of power quality is becoming increasingly important. An effective way for harmonic suppression is the harmonic compensation by using active power filter. This paper presents a comprehensive survey of DSTATCOM and is aimed at providing a broad perspective on the status of DSTATCOM control methods to researchers and application engineers dealing with harmonic suppression issues. Many control techniques have been designed, developed, and realized for active filters in recent years. This paper presents different types of Synchronous reference frame methods for real time generation of compensating current for harmonic mitigation and reactive power compensation. All the techniques are analyzed mathematically and simulation results are obtained which are being compared in terms of its compensation performance with different parameters under steady state condition. Shunt compensation for medium voltage distribution systems requires higher rating for voltage source converters (VSCs). Ratings of the semiconductor devices in a VSC are always limited; therefore, for higher rated converters it is desirable to distribute the stress among the number of devices using multilevel topology. Cascaded multilevel configuration of the inverter has the advantage of its simplicity and modularity over the configurations of the diode-clamped and flying capacitor multilevel inverters. Application of cascaded multilevel converters for shunt compensation of distribution systems has been described in Literature. This paper presents an investigation of five-Level Cascaded H – bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package. The proposed DSTATCOM is simulated for both linear and nonlinear loads.*

**Keywords- DSTATCOM, Power Quality Level Shifted Pulse Width Modulation (LSPWM), Phase Shifted Pulse Width Modulation (PSPWM), Proportional-Integral (PI) Control.**

## I. INTRODUCTION

One of the most common power quality problems today is voltage dips. A voltage dip is a short time (10 ms to 1 minute) event during which a reduction in r.m.s voltage magnitude occurs. It is often set only by two parameters, depth/magnitude and duration. The voltage dip magnitude is ranged from 10% to 90% of nominal

voltage (which corresponds to 90% to 10% remaining voltage) and with a duration from half a cycle to 1 min. In a three-phase system a voltage dip is by nature a three-phase phenomenon, which affects both the phase-to-ground and phase-to-phase voltages. A voltage dip is caused by a fault in the utility system, a fault within the customer's facility or a large increase of the load current, like starting a motor or transformer energizing. Typical faults are single-phase or multiple-phase short circuits, which leads to high currents. The high current results in a voltage drop over the network impedance. At the fault location the voltage in the faulted phases drops close to zero, whereas in the non-faulted phases it remains more or less unchanged [1, 2]. Voltage dips are one of the most occurring power quality problems. Off course, for an industry an outage is worse, than a voltage dip, but voltage dips occur more often and cause severe problems and economical losses. Utilities often focus on disturbances from end-user equipment as the main power quality problems. This is correct for many disturbances, flicker, harmonics, etc., but voltage dips mainly have their origin in the higher voltage levels. Faults due to lightning, is one of the most common causes to voltage dips on overhead lines. If the economical losses due to voltage dips are significant, mitigation actions can be profitable for the customer and even in some cases for the utility. Since there is no standard solution which will work for every site, each mitigation action must be carefully planned and evaluated. There are different ways to mitigate voltage dips, swell and interruptions in transmission and distribution systems. At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications [3, 4]. Among these, the distribution static compensator and the dynamic voltage restorer are most effective devices, both of them based on the VSC principle. The STATCOM used in distribution systems is called DSTACOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a DSTATCOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

## II. DESIGN OF MULTILEVEL BASED DSTATCOM

### 2.1 Principle Of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure-1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the

DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

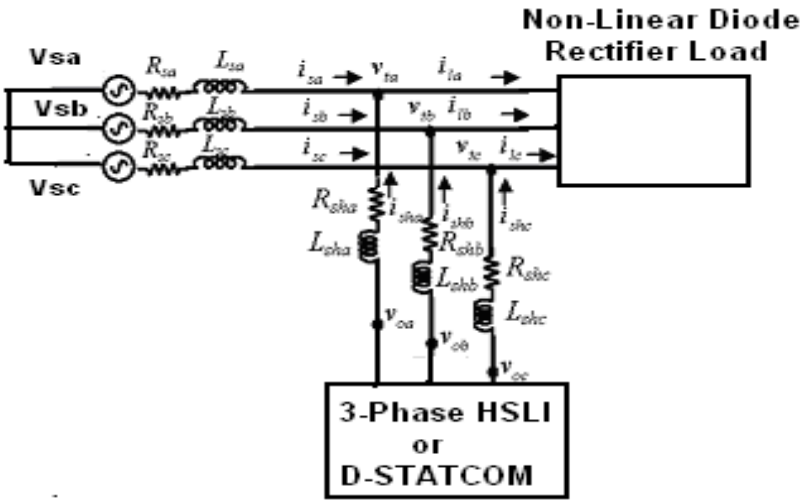


**Figure – 1 Schematic Diagram of a DSTATCOM**

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

### 2.1 Control For Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

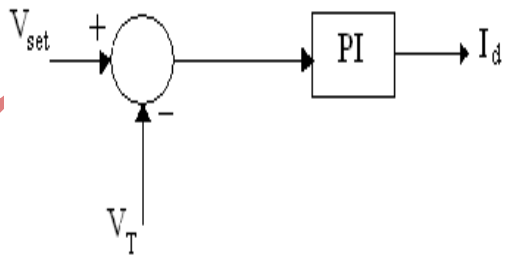


**Figure-2 PI Control For Reactive Power Compensation**

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and

generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

### 2.3 Control For Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (id-iq) method. This is similar to the Synchrous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V (a,b,c) and the available currents $i_l$ (a,b,c) in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where '0' represents the instantaneous voltage vector angle (5).

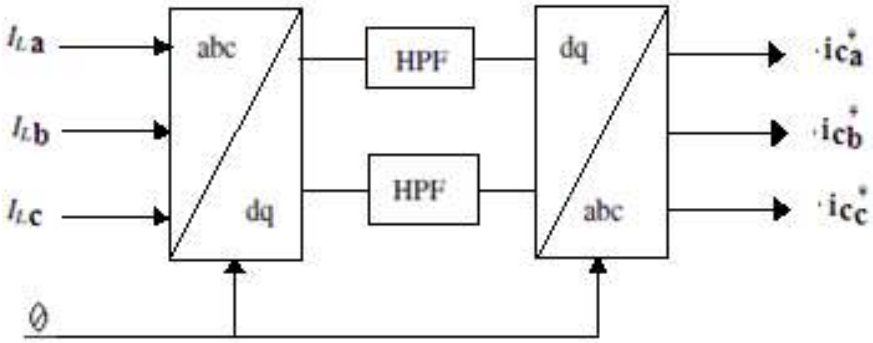


**Figure-3 Block diagram of SRF method**

| Switches Turn ON | Voltage Level |
|---|---|
| S1,S2 | Vdc |
| S3,S4 | -Vdc |
| S4,D2 | 0 |

**Table-1 Switching table of single CHB inverter**

### 2.4 Cascaded H-Bridge Multilevel Inverter

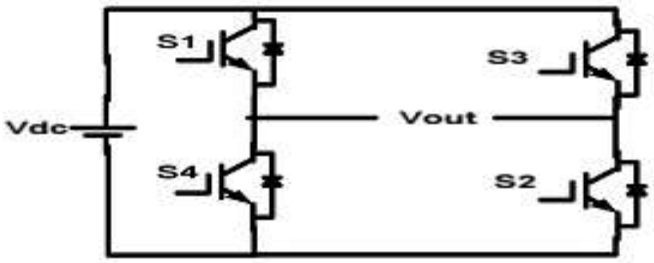


**Figure-4 Circuit of the single cascaded H-Bridge Inverter**

Fig.4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is

given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

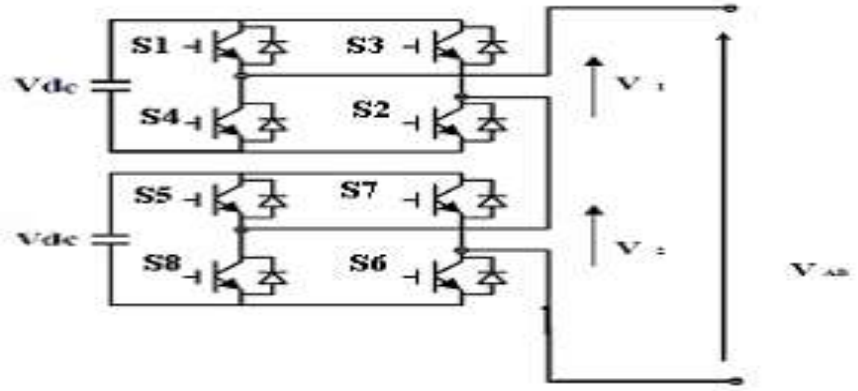


**Figure-5 Block diagram of 5-level CHB inverter model**

The switching mechanism for 5-level CHB inverter is shown in table-2.

**Table 2.Switching table for 5-level CHB Inverter**

| Switches Turn On | Voltage Level |
|---|---|
| S1, S2 | Vdc |
| S1,S2,S5,S6 | 2Vdc |
| S4,D2,S8,D6 | 0 |
| S3,S4 | -Vdc |
| S3,S4,S7,S8 | -2Vdc |

### 2.5 PWM Techniques For CHB Inverter

The most popular PWM techniques for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM).

### 2.1.1 Phase Shifted Carrier PWM (PSCPWM)

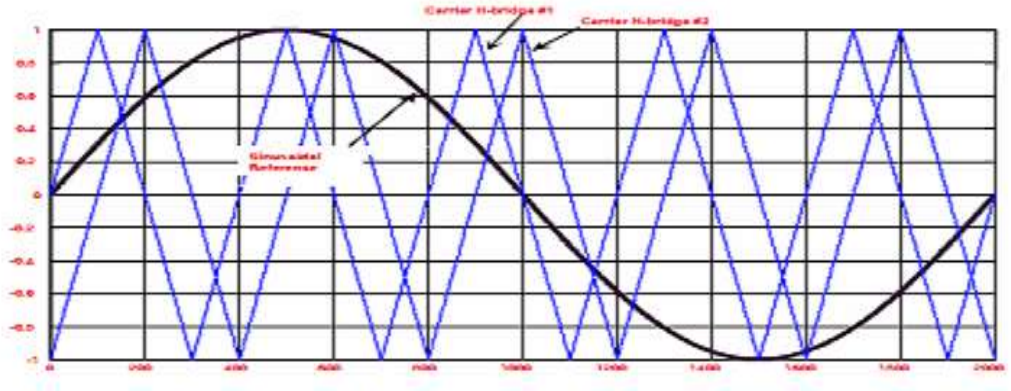

**Fig. 6 phase shifted carrier PWM**

Fig6 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

### 2.1.2 Level Shifted Carrier PWM (LSCPWM)

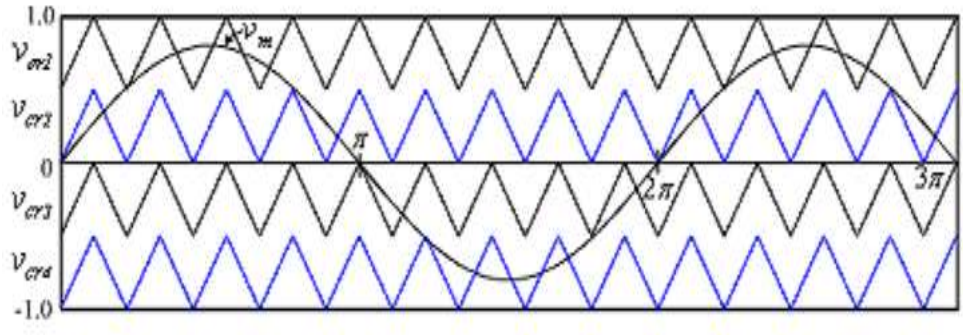


**Fig.7 Level shifted carrier PWM**

Fig.7 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by 1/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

## III. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Here Matlab/Simulink modle is developed for two cases. In case one DSATCOM with Linear load and in case two DSTATCOM with nonlinear load are simulated.

### 3.1 Case One

Fig8 shows the Matab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block.

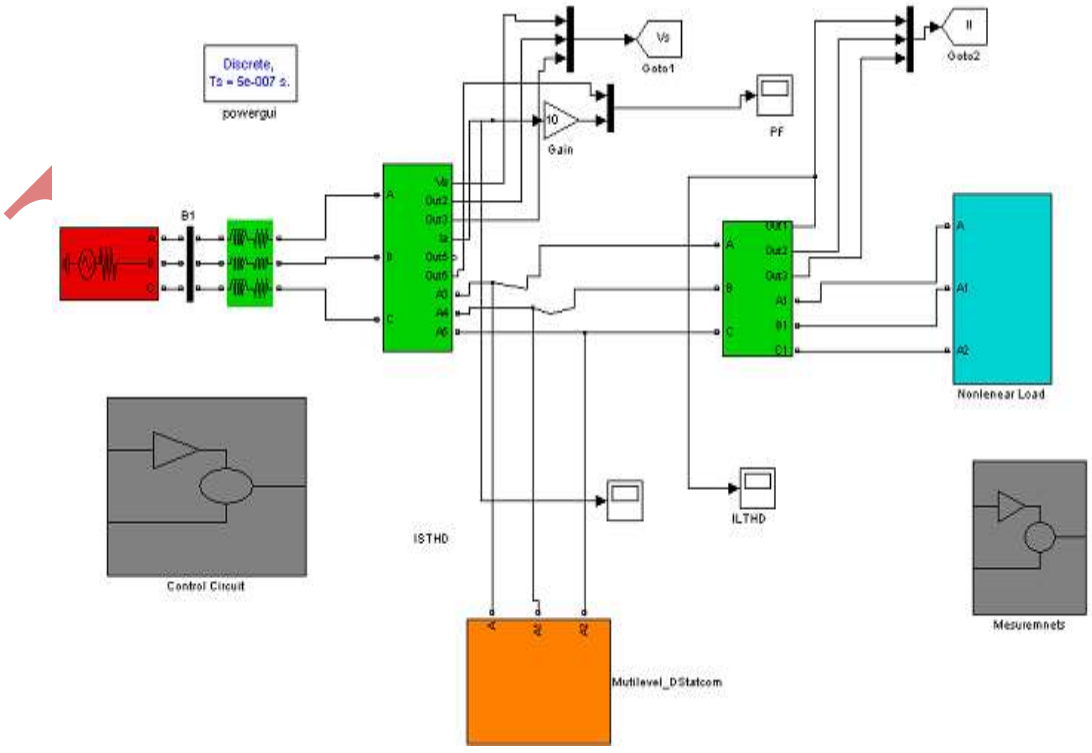


**Fig. 8 Matlab/Simulink power circuit model of DSTATCOM**

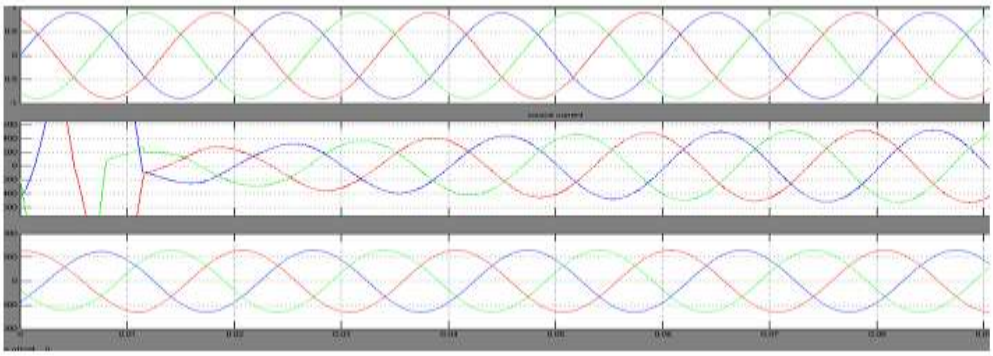

**Fig. 9 Source Voltage, Current And Load Current With DSTATCOM**

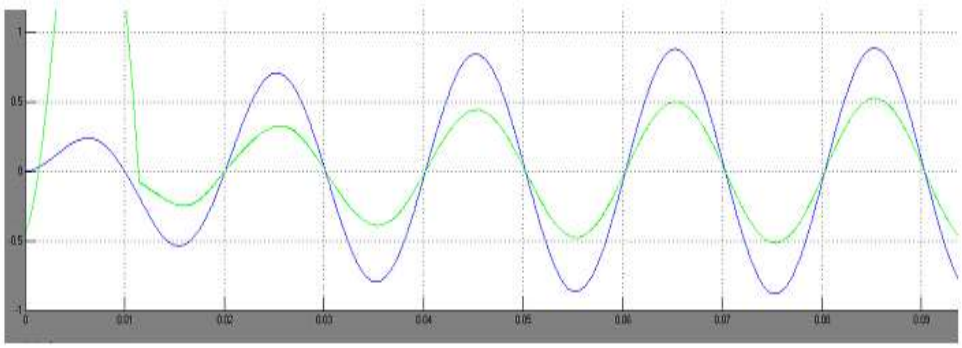

**Fig.10 Phase-A Source Voltage And Current**

Fig.10 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

### 3.2 Case Two

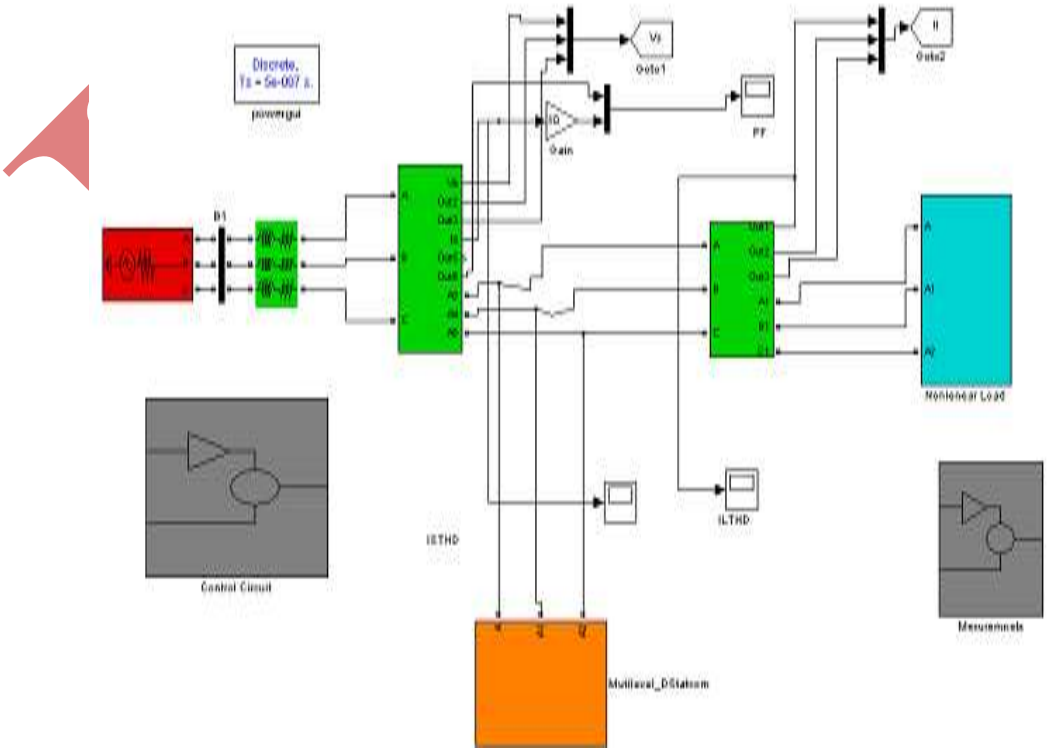


**Fig.11 Matlab/Simulink Power Circuit Model Of DSTATCOM**

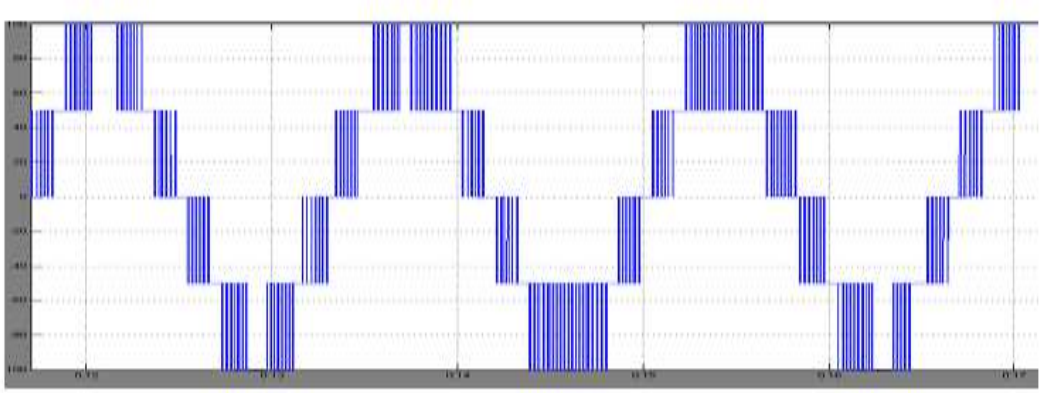

**Fig. 12 five levels PSCPWM output**

Fig. 13 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

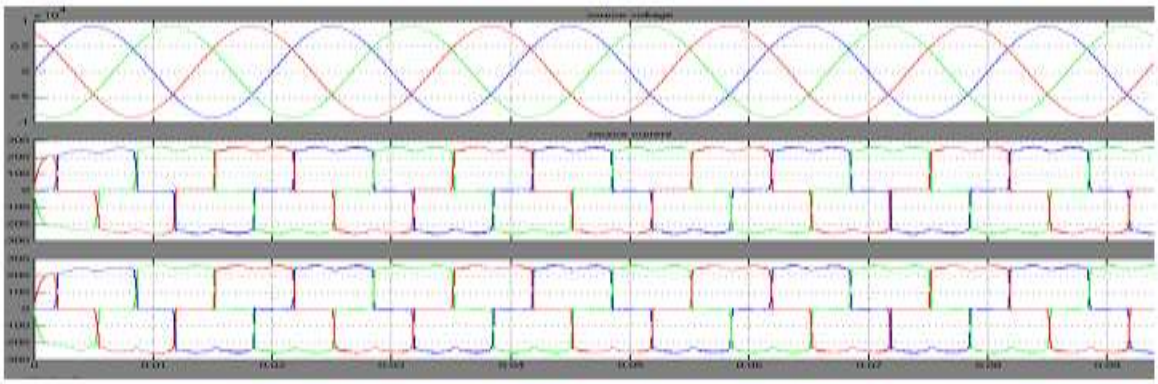

**Fig. 13 Source voltage, current and load current without DSTATCOM**

Fig. 14 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

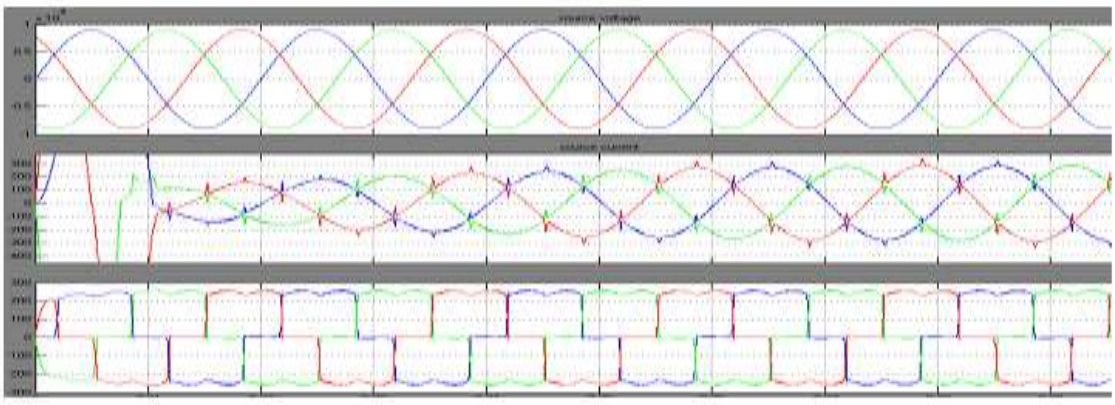

**Fig. 14 Source voltage, current and load current with DSTATCOM**

Fig. 15 shows the DC bus voltage. The DC bus voltage is regulated to 11kv by using PI regulator.

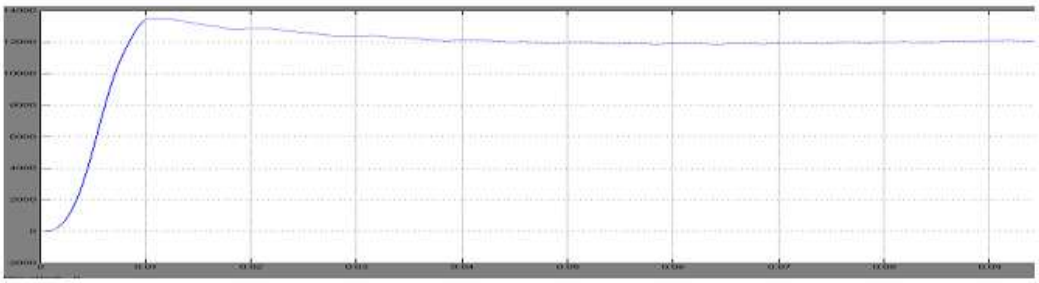

**Fig. 15 DC Bus Voltage**

Fig. 16 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

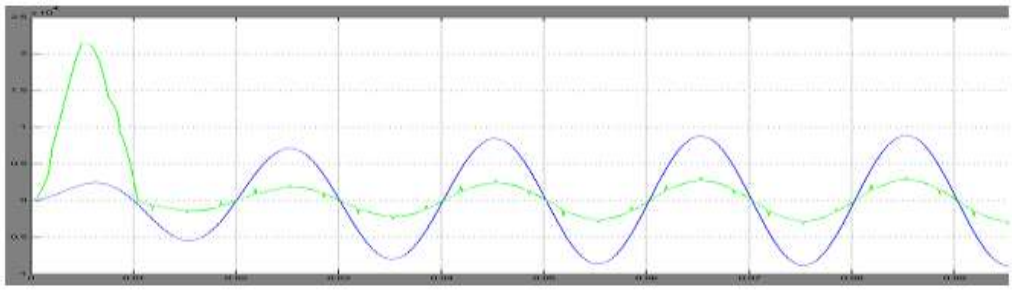

**Fig. 16 Phase-A source voltage and current**

Fig. 17 shows the harmonic spectrum of Phase –A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

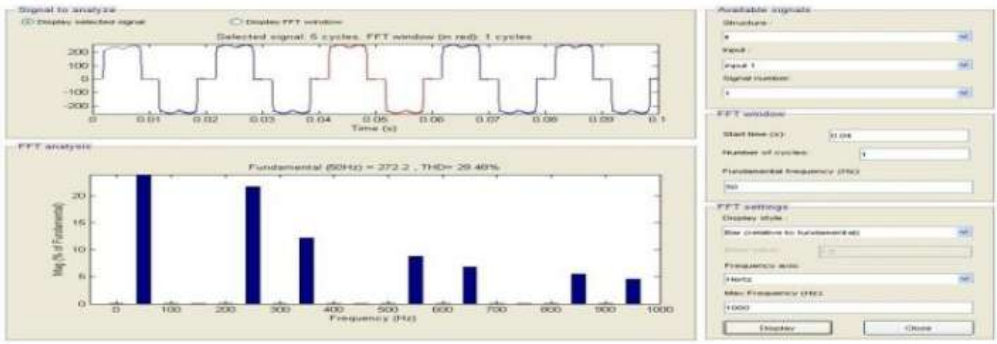

**Fig. 17 Harmonic spectrum of Phase-A Source current without DSTATCOM**

Fig. 18 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current without DSTACOM is 5.05%

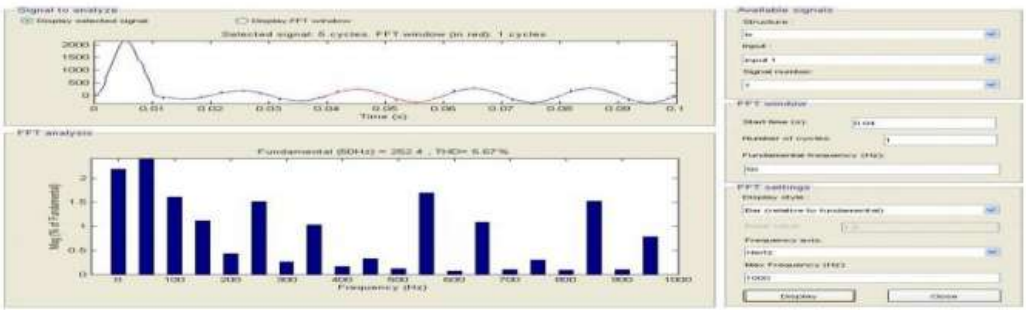

**Fig. 18 Harmonic spectrum of Phase-A Source current with DSTATCOM**

## IV. CONCLUSION

This paper studied a five level inverter used in a DSTATCOM in PS and has been successfully demonstrated in MatLab/Simulink. The befits of five level inverter has low harmonics distortion, reduced number of switches to achieve the seven- level inverter output over the cascaded seven level inverter and reduced switching losses. A DSTATCOM with five levels CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage , load voltage , source current, load current, power factor simulation results under non-linear loads are presented. Finally Matlab/Simulink based model is developed and simulation results are presented for both linear and non linear loads.

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