INVESTIGATION OF FREQUENCY DEPENDENCE ON THE NOISE RESPONSE OF A NOVEL TRANSPARENT GATE RECESSED CHANNEL MOSFET

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ABSTRACT

The noise assessment of Novel Transparent Gate Recessed Channel MOSFET has been investigated based on the simulated result from ATLAS device simulation. TCAD simulation results show TGRC-MOSFET divulges Conventional Recessed Channel (CRC)-MOSFET in terms of reduction in noise figure, cross correlation, noise conductance and parasitic capacitances. It also achieves higher optimum source impedance for high performance applications where noise immunity is a key factor.

Keywords: ATLAS, CRC-MOSFET, noise, optimum impedance, paracitic capacitance, TGRC MOSFET.

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I. INTRODUCTION

Field Effect Transistor (MOSFET) sizes close to their physical limits. CMOS technology is being used for the designing Linearity of RF amplifier is an important factor for use in digital communication. Application of RF circuits need transistor with minimum intermodulation distortion and noise [1]. Advancements in semiconductor manufacturing techniques and to achieve high speed and more packing density, complicated Integrated Circuits (ICs) have driven the associated Metal Oxide Semiconductor of circuits for super high frequencies communication. Scaling-down of MOS devices improves RF performance characterstics. On the other hand, it is difficult to scale-down the supply voltage used to perform these ICs consistently due to compatibility problem with earlier generation circuits, noise margin, power and delay requirements, but not scaling of subthresold slope and threshold voltage. While the successive increase in internal electric fields in aggressively scaled MOSFETs comes with the additional ameliorate of increased carrier velocities, and hence increased switching speed, it also presents higher reliability complications for the long period of operation of these devices [2]. As the size and signal levels of a MOSFET is scaled-down, the low frequency noise (LFN) properties become more important as the LFN is higher than the signals [3-4].

To abate the noise effects in CRC-MOSFET, instead of metallic gate, Indium Tin Oxide has been used. Indium tin oxide (ITO or tin-doped indium oxide) is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is colorless and transparent in thin layers. Indium tin oxide is one of the most widely used transparent conducting oxides because of its two leading properties, its optical transparency and electrical conductivity , as well as the ease with which it can be deposited as a thin film [5]. The In_2O_3 phase itself contributes free electron for electrical conductivity [6-8]. When Tin (Sn) is diffused, then some of the oxygen vacancies may be created by SnO_2 which creates free electrons to enhance the concentration of carriers and hence increase conductivity and decrease the resistivity with temperature. As the device scales-down, parasitic capacitances arises. These parasitic capacitances degrade the device performance. By using TGRC-MOSFET, parasitic capacitances can be reduced significantly.

II. DEVICE STRUCTURE AND ITS PARAMETERS

The simulation device structure i.e. Transparent Gate Recessed Channel MOSFET consists of gate which is made by transparent conducting material Indium Tin Oxide (ITO) as shown in Fig 1. The total gate length is 30 nm and thickness of oxide is 2.0 nm. Groove depth is 38 nm and source/drain junction depth is 30 nm. Here we have taken negative junction depth 10 nm.

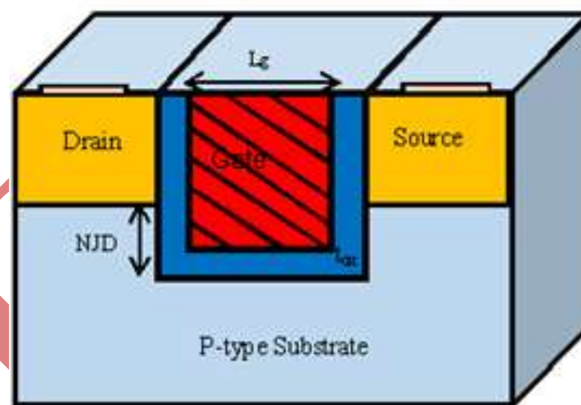

Fig. 1: Structure of Transparent Gate Recessed Channel MOSFET.

Gate to source and drain to source voltage is 0.7 V. Workfuntion taken for transparent material is 4.7 eV in TGRC-MOSFET and 4.1 eV for metal in CRC-MOSFET. All simulations have been performed using ATLAS device simulator. The simulations are based on the inversion layer Lombardi CVT mobility model with the Auger recombination model and Shockley-Read –Hall (SRH) for minority carrier recombination. Further the hydrodynamic energy transport model comprising of the continuity equations, energy balance equations of the carriers, momentum transport equations and Poisson’s equation have also been enabled [9].

III. TCAD SIMULATION RESULTS OF TRANSPARENT GATE RECESSED CHANNEL MOSFET

The present analysis is carried out for a channel length, L_G=30nm, uniformly doped source/drain, N_D with doping density of $1x10^{19}$ cm^{-3}, p type substrate doping, N_A with a doping density of $1x10^{17}$ cm^{-3}, SiO_2 thickness, t_{ox}=2.0 nm. The gate work function (Φ_{ITO}) is 4.7 eV.

3.1 Minimum Noise Figure

Noise figure is generally used as a measure of an amplifer's RF performance. Fig.2. shows the minimum noise figure for CRC-MOSFET and TGRC-MOSFET at different frequencies. When frequency increases from 100 Hz to 10 GHz, minimum noise figure decreases in TGRC-MOSEFT compared to CRC-MOSFET.

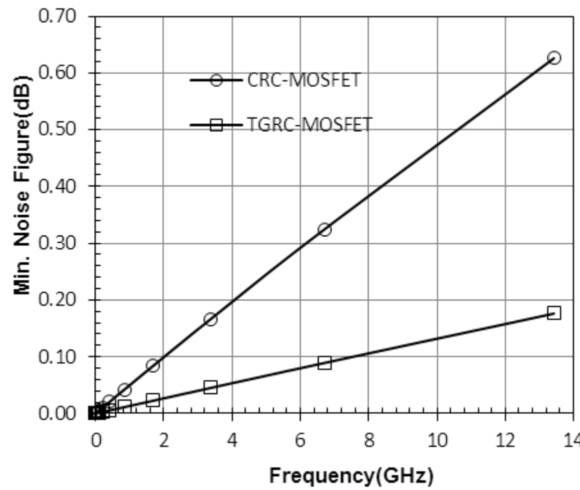

Fig. 2: Minimum noise figure for CRC- MOSFET and TGRC-MOSFET.

The observation is mainly attributed to the transparent conducting material in the TGRC-MOSFET architecture because in transparent material, random motion of free electrons decreases. In transparent conducting material, the temperature rise is not much significant when concentration of charge carriers is increased, due to which noise figure decreases.

3.2 Optimum Source Impedance

Fig.3. predicts the behavior of optimum source impedance ($Z_{OPT}=R_{OPT}+jX_{OPT}$) with respect to frequency. When the frequency increases, optimum impedance decreases in CRC-MOSFET while it is maximum at low frequencies.

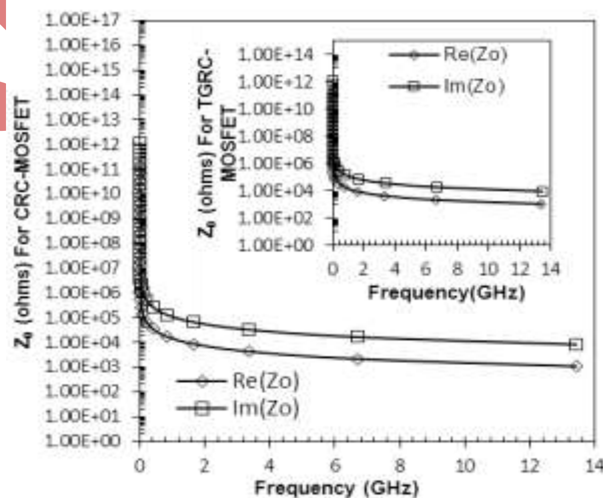

Fig. 3: Optimum source impedance Z_0 for CRC-MOSFET. Inset- Optimum source impedance Z_0 for TGRC- MOSFET.

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As evident from Fig.3, the optimum source impedance in TGRC-MOSFET is slightly higher than CRC-MOSFET because of the presence of indium tin oxide in TGRC-MOSFET which is effectively acting as a parallel oxide with SiO_2 and hence effective permittivity is increased which eventually leads to increase in input impedance. This high impedance of TGRC-MOSFET also helps in reduction of electrostatic charges, which basically comes in to existence with scale-down of oxide [10].

3.3 Parasitic Capacitance

In addition, for better performance of a device in microwave-communication, parasitic capacitances should be as small as possible. Local stress on the radio-frequency (RF) performance of the transistor and parasitic capacitances are investigated in 30-nm CMOS technology [11]. Parasitic capacitances and resistance put upper limit on the speed of a transistor [12].

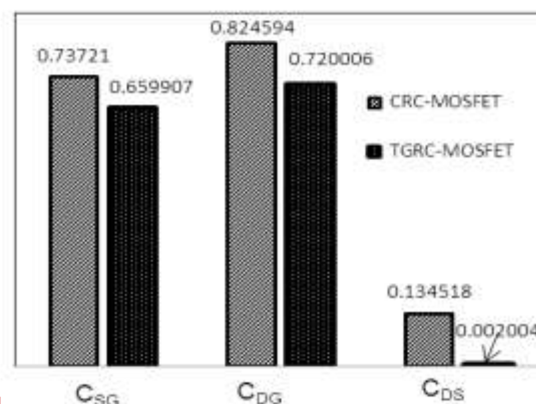

Fig. 4: Parasitic capacitance (femto-Farad) for CRC- MOSFET and TGRC-MOSFET.

Parasitic capacitance is the cause of delay in logic-cell. When one logic cell drives another, the parasitic input capacitance of the driven cell becomes the load capacitance of the driven cell [13]. Fig.4 shows that the parasitic capacitances in TGRC-MOSFET are less than the CRC-MOSFET. The ITO-SiO_2 forms a MOS capacitor with ITO serving as metallic gate electrode at GHz frequencies and SiO_2 forming the gate insulator [14].

3.4 Noise Conductance

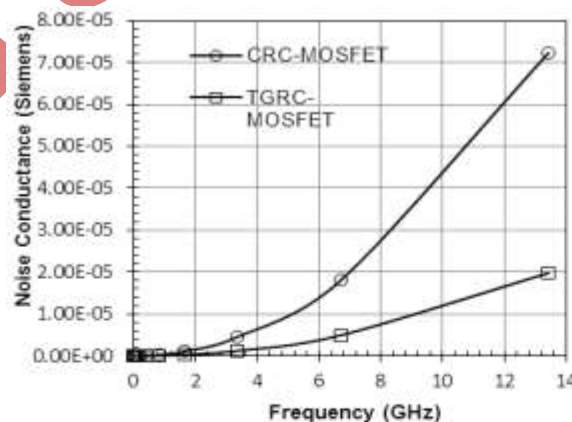

Fig. 5: Noise conductance for CRC- MOSFET and TGRC-MOSFET.

Further, in the RF applications of a MOS device, noise conductance should be as low as possible. In a MOS device, noise conductance increases due to thermally generated charge carriers. In TGRC-MOSFET, noise conductance is low because in transparent conducting material, oxygen vacancies created by oxides give more free electrons and hence, mobility decreases with increase in the concentration of charge carriers, leading to lesser number of thermally generated charge carriers as is shown in Fig.5.

3.5 Cross Correlation

Here, MOSFET is considered as a two port device as shown in Fig.6 i.e. the noise induced at the gate terminal is separated from the MOSFET and is represented by V1 and the noise received at the output is replaced by a voltage V2 [15]. Some statistical analysis is obligatory for this research since noise is a random phenomenon. Thus, cross correlation of the voltages at the two port of the device is compared. It is clearly evident from Fig.7 that cross correlation in TGRC-MOSFET is lower as compared to CRC-MOSFET at GHz frequencies.

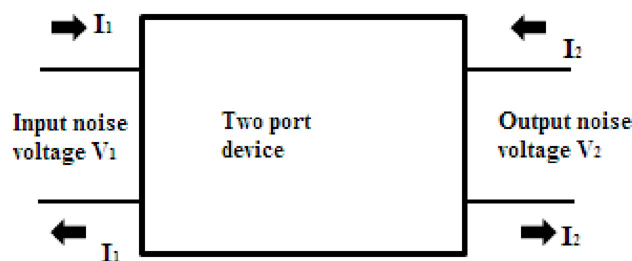

Fig. 6: MOSFET as a two port device where the input noise is replaced by a voltage V1 and the noise received at output is replaced by V2.

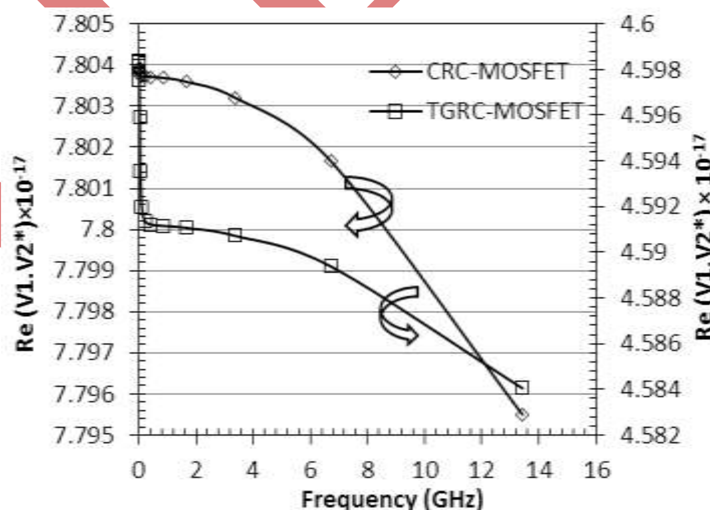

Fig. 7: Cross correlation for CRC- MOSFET and TGRC-MOSFET.

In TGRC-MOSFET electric field is lower at the drain side. Therefore, isotropic scattering reduces and mean free path (λ) of carriers crossing the channel (as a function of frequency) is much larger than CRC-MOSFET [6] due

to transparent gate and reduced surface scattering at the Si-SiO_2 interface. Due to this reduced isotropic scattering, the scattering mechanism is not so effective in breaking the correlation between gate current and drain current [15]. Thus, cross correlation (i.e. V1.V2*) reduces in TGRC-MOSFET at higher frequencies.

IV CONCLUSION

In this work, we focused on Transparent Gate incorporation onto the Conventional Recessed Channel MOSFET for superior noise performance of scaled MOS devices. TCAD simulation reveals reduction in minimum noise figure, noise conductance and parasitic capacitances for TGRC-MOSFET. It also achieves higher optimum source impedance. Hence TGRC-MOSFET is a reliable solution for RF applications and CMOS technology for the designing of multi-gigahertz communication circuits.

V. ACKNOWLEDGMENT

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